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SYMMETRY PATTERN RECOGNITION SYSTEM II

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ABSTRACT

Automatization of satellite detection in the SPASUR system requires a means of discriminating against a large population of nonsatellite responses. Early in the program, a study of SPASUR automatic gain control (agc) amplitude responses led to the development of a pattern recognitions system based upon the inherent symmetry of a typical signal due to a satellite pass.

This report describes the developed recognition system, called the Symmetry Recognition System II. The technical performance of the equipment placed in operation at the San Diego Space Surveillance Station (SPASURSTA) in November 1961 is presented. During a ten-hour period on November 6, 106 alerts were generated, of which 20 were satellites which were correctly called symmetrical and 39 were nonsatellites which were rejected. Symmetry responses were generated on 14 alerts, some of which may have been due to remote, unverified satellite passes. No symmetry response was given to 33 verified satellites. Seven of these passes were missed due to agc pattern distortion by the SPASUR comb-filter switching action. Of the remaining signals, 25 were below the agc noise level and could not be examined for symmetry, and one low-level, short response was missed due to rapid signal fluctuations.

It is concluded that recent design advances in the SPASUR system have minimized the requirement for pattern recognition processing.

PROBLEM STATUS

This report completes this phase of the problem. Work on other phases of the problem continues.

AUTHORIZATION

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SYMMETRY PATTERN RECOGNITION SYSTEM II

BACKGROUND

Efforts to automatize the manual evaluation of signals in the SPASUR satellite detection system require a means of distinguishing between valid responses and a large population of returns due to meteors, their ionized trails, aircraft, and other anomalies of the atmosphere or the ionosphere, whether natural or artificial. SPASUR satellite-bounce signals are presented in two forms: a set of phase signals representing the space angle from which a satellite signal is received, and automatic gain control (agc) signals proportional to the amplitudes of the signals received in the phase measuring system.

The phase channel signals are each characterized by random noise in the absence of any coherent signal, the amplitude of which reduces to essentially a dc signal value during a satellite passage. Since space angles are to be automatically computed in real time from these dc values, supplementary means are necessary to validate the presence of signals of interest. The quieting of the phase channels is one means which could be used in identifying the period or event when the space angle measurement is to be accepted. Further evaluation and confirmation is necessary before this event can be labeled as due to a satellite, with a high degree of probability (or with an acceptably low false-alarm rate). Simultaneous signals at two receiving stations are a reasonably reliable indication of a satellite pass. The measurement of phase and the rate of change of phase can be applied as a further aid in the recognition of satellite-type signals. Information on frequency shift due to doppler is available in the SPASUR alert system as a by-product of the comb-filter operation.

The analysis of the agc signal offers a positive correlation factor in the identification of characteristics associated with true satellite passes. A study of numerous verified satellite agc signatures reveals a symmetrical contour approximating the cosine squared pulse, or sin x/x form. Nonsatellite signals have nonsinusoidal patterns in most instances, thus offering the opportunity for discriminating between the desired and undesired signals. Some of the possible approaches to the recognition of these patterns include the analysis of the signals' harmonic contents, the normalization of amplitude and duration, and tests for symmetry. This report concerns the development of a symmetry recognition system acting upon the SPASUR agc signal.

Although amplitude-vs-time recordings of agc signals due to satellite passes are basically symmetrical on each side of a line drawn perpendicular to the time axis through the peak, as in Fig. 1(a), a number of signal variables influence the design of a system to carry out automatic recognition. Perturbations of the signal will be caused by rotation of the satellite, modulating the reflected signal when resonant antenna elements or specular surfaces cause reinforcement or cancellation. Faraday rotation effects may produce variations in the polarization plane. These factors may distort the satellite signature as in Figs. 1(b) and (c). In Fig. 1(d), reflections from meteor trails can distort the symmetry of a satellite echo, although such occurrences are relatively infrequent. Reflections from aircraft over the transmitter may produce signatures having one or more lobes, each resembling a satellite pass as in Fig. 1(b), but normally of greater duration. A symmetry recognition system should be able to accommodate these responses to the degree that a material reduction can be effected in the nonsatellite signals which need be processed by the data link and the computer.

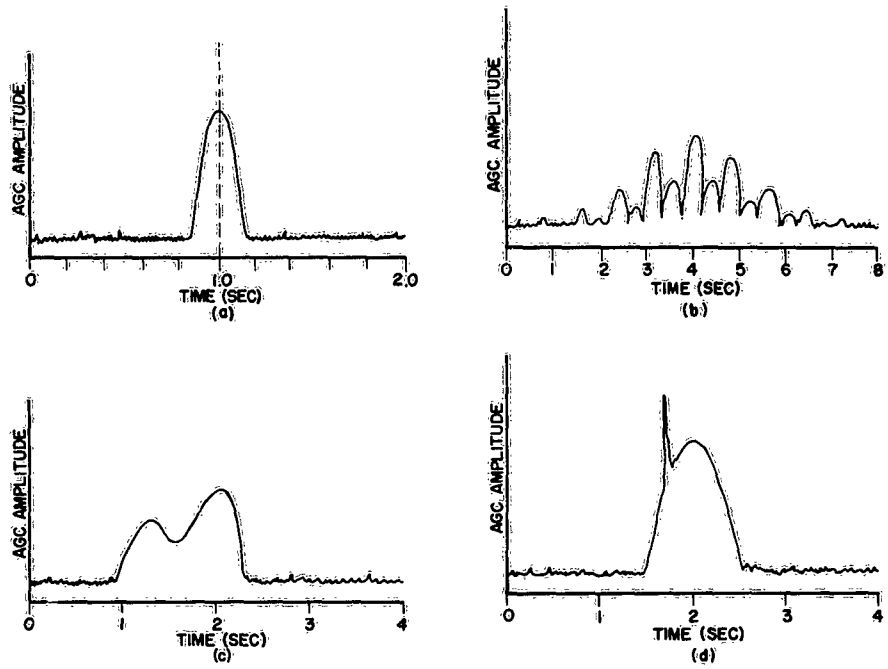


Fig. 1 - Typical wideband SPASUR agc responses to satellite passes: (a) illustration of the fact that all responses are basically symmetric around the peak amplitude; (b) representative radiating satellite signal; (c) distorted agc signal due to overlapping of nearly simultaneous satellite passes; and (d) satellite response distorted by meteor reflection

Pattern recognition is one method considered for use in identifying a satellite signal at the receiver. Other methods applicable at the central processor include the use of triangulation, the measurement of doppler shift and space angle, and the correlation with orbital elements of known satellites. Each contributes to a combined measure of probability that a satellite has been observed.

SYMMETRY RECOGNITION TECHNIQUE CONSIDERATIONS

In order to measure the point-to-point pattern symmetry of a waveform, a means of signal storage is required. Magnetic recording was first considered, but the frequencies of interest may be as low as 0.1 cps, well below the direct-recording low-frequency limit of about 30 cps. By using the signal to frequency-modulate a suitable carrier, recordings can be made from dc up to at least 10 percent of the carrier frequency. A more serious problem is the need for a means of rapidly and repetitively scanning the stored waveform simultaneously both forward and backward in time, starting at the midpoint of the recording. The scanner outputs would then be followed by the symmetry recognition circuitry. This would require considerable mechanical development work to provide properly synchronized contrarotating reproducer heads. Mechanical wear of both the tape recording media and the recorder scanning mechanism would be appreciable, since continuous operation is necessary.

An all-electronic system, to avoid the mechanical problems of a magnetic tape recorder, is feasible in either the digital or analog form. A study of the range of satellite response signal values indicates a nominal duration of from 0.2 second to 5 seconds and an amplitude range representing 40 db of agc. Figure 2 represents a characteristic satellite response stored in a 100-element delay line. A practical minimum number of discrete periods to be examined for amplitude symmetry over each half of a 0.2-sec signal is approximately five. By extending the examination period to about two seconds, while retaining this same resolution, both the shortest and a significant portion of the longer signals can be included in one recognition system which stores 100 contiguous 0.02-sec quantizations of the input.

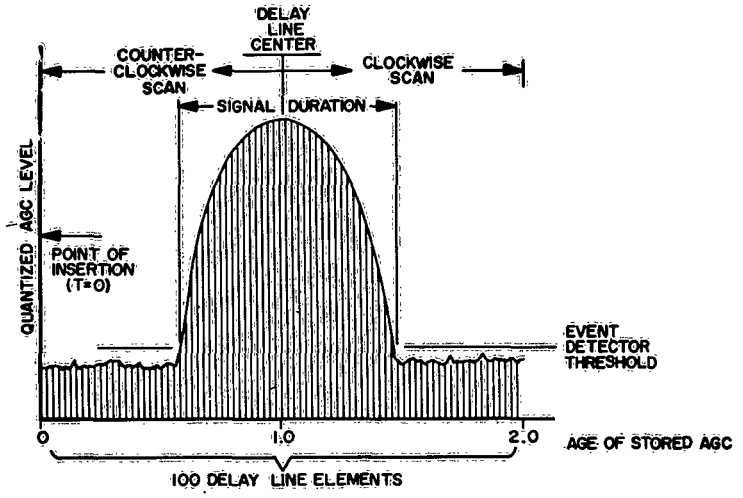


Fig. 2 - Characteristic satellite response stored in 100-element delay line

A digital system to accomplish this could be arranged as in Fig. 3. An analog-to-digital converter (ADCON) having a minimum resolution of eight binary digital bits, and possibly as many as ten bits, provides a continuous conversion of an agc channel. The eight ADCON bits are connected to a magnetic drum, or an electronically rotating store, by way of a like number of gates which are controlled by a programmer. The store would contain a minimum of 100 eight-bit words and would be caused to rotate with respect to the readin/readout point at a rate of 50 rps as determined by the clock-driven programmer. Under these conditions, the clock rate would be 5 kc. Extending the storage to 10 seconds and doubling the time resolution to 0.01 second would increase the store to 1000 words and the clock rate to 10 kc. Requiring the store to rotate once for each new word inserted permits the insertion point to be arbitrarily located. The programmer then times the insertion of each new word into the store so that at the "read" output the even-numbered sequence of words will be scanned "forward" or "clockwise" in time, while the odd sequence is scanned "backward" or "counterclockwise." Upon readout, successive pairs of words are subtracted digitally, and the magnitude of the remainder represents the degree of asymmetry. At this point, a simple threshold decision based upon the absence of any binary digit greater than some predetermined value 2^k, where $0 > k > n$ would give a measure of the symmetry. This operation is continued, examining every word pair in the store for

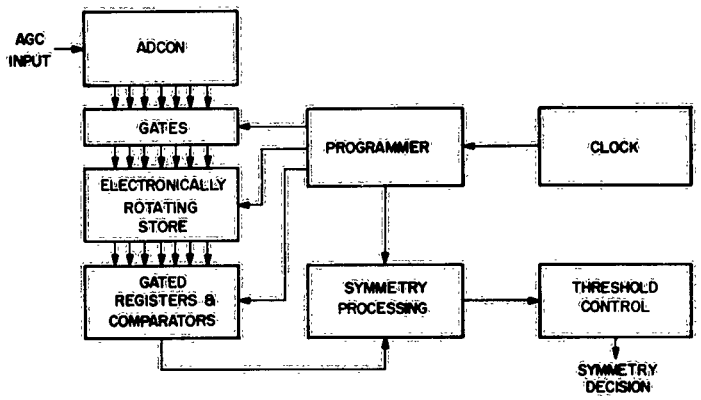


Fig. 3 - Symmetry Recognition System, digital method

every complete store rotation. A counter, advancing once for each positive indication of symmetry, provides an integrated measure of the degree of symmetry over the entire scan (one rotation of the store), at the end of which the accumulated count is read out and the counter is reset to zero.

An analog system, based upon the block diagram in Fig. 4, was chosen for development. The processing steps are quite similar to those shown in Fig. 3, with the electronically rotating digital store being replaced by a delay line capable of storing a real-time advancing series of dc analog signal values, all of which are continuously available for repetitive scanning. Many factors, such as the cost and procurement time required for an electronically rotating digital store, the availability of analog storage and gating designs, and the flexibility, resolution, and economy of analog function-forming techniques, dictated the choice of analog methods for the developmental model. Once such factors as the optimum length and resolution of a delay line, the character of the signal processing, and the nature of the threshold controls have been established through extended in-service experience, a corresponding digital system specification could be prepared. Where the number of analog stores (equivalent to words in the digital system) exceeds 100 by an appreciable amount, the virtually linear increase in costs and size of the analog system begin to surpass the more nearly fixed costs of the digital ADCON, rotating store, and programmer.

Whether analog or digital methods are chosen, several occurrences not associated with a satellite pass may contribute to a level of symmetry indication which would also be present with the transit of a true satellite. The normal background level in the delay line is symmetrical since it approximates a straight line at every time interval, but the response to this condition is suppressed by an internal scanner threshold and also by the SPASUR comb-filter system threshold gate which permits an alert pulse to be generated only when the agc signal-to-noise ratio exceeds 13 db. Calibrate signals are regularly introduced into the rf portion of the SPASUR system. These are detected as square waves which are symmetrical, but since they are predictable, a response to these events can be inhibited. Step-function shifts in the dc level of the agc lines can occur with manual system adjustments, or variables in the performance of the electronics. Level-correcting techniques are incorporated to normalize the agc signals against most anomalies which may be encountered. The remaining nonsatellite signals which occasionally show symmetry are lightning discharges, overdense meteor trails, and responses from the moon, sun, and radio stars.

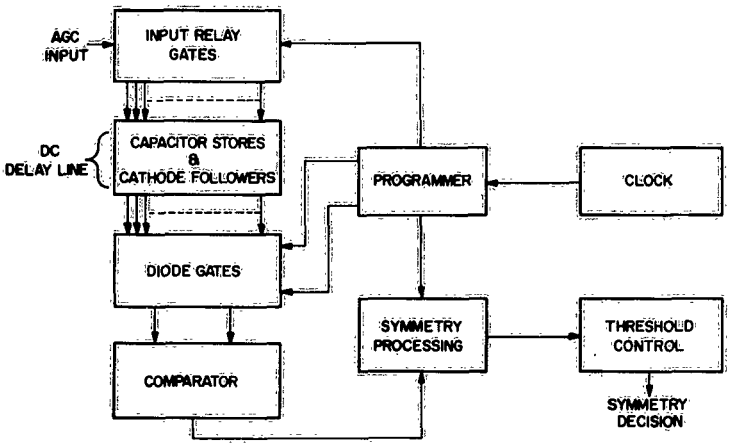


Fig. 4 - Symmetry Recognition System, analog method

Time thresholds are useful in reducing the number of responses to nonsatellite sources. Requiring the SPASUR Alert signal to persist for 0.2 second before enabling the symmetry threshold output to transmit a recognition pulse permits the exclusion of shorter meteor and random-noise symmetry responses without losing satellite responses, since satellite signals normally exceed this lower limit.

ANALOG TECHNIQUE APPROACH

Based largely upon the scanning and storage techniques described in Ref. 1, the Symmetry Recognition System configuration shown in Fig. 5 was proposed. The SPASUR Alert agc, which is derived from the comb-filter channels, is chosen in preference to the agc of the phase channel gated by the alert signal since the former should always contain more of the rise and fall times of the signal, especially the critical short-duration signals in the vicinity of 0.2 second. Early samples of the phase channel agc showed considerable amplitude distortion due to the rapid random switching action of the comb filter. This signal is fed to the poles of 100 mercury-wetted contact relays, chosen because of their 2-ms operating speed and their excellent contact reliability under "dry-circuit" conditions. Each relay output contact is connected to a low-loss 0.1-mfd storage capacitor so that when the relay is pulsed, the capacitor will be charged to the value of the agc appearing on the pole at that instant. By sequentially pulsing each relay at 20-ms intervals, a 2-sec record of the signal is stored as 100 quantized levels. The potential at each capacitor is measured by a low-grid-current cathode follower, permitting each of the capacitors to be measured without disturbing the stored values. During the capacitor charging period, the associated cathode follower is included within the feedback loop of the insertion driver amplifier in order to correct for its bias and gain errors.

Electronic switches are programmed to sample pairs of cathode followers, beginning each cycle with those followers connected to capacitors 49 and 50. Capacitor number 1 represents the capacitor storing the most recent agc value, and number 100 represents the value two seconds into the past. After 200 microseconds, capacitors 49 and 50 are switched off and the next pair, 48 and 51, are activated for a like period. Continuing in this manner for 50 operations over a 10-ms period brings the two scanners to the outputs of numbers 1 and 100, respectively, thus completing one scan of the stored signal. The outputs of these two gates become inputs to a comparator, which will give a standardized

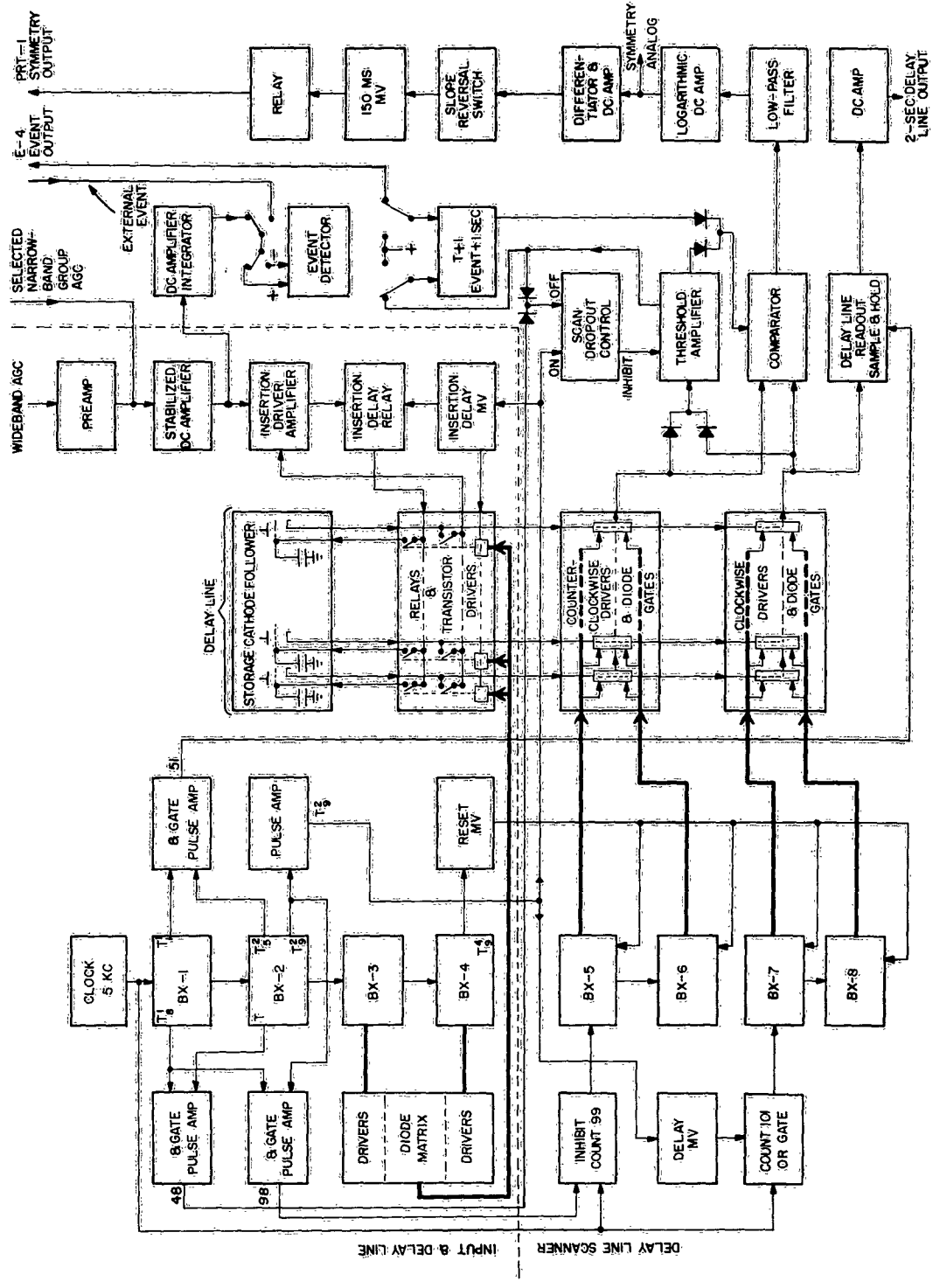


Fig. 5 - Symmetry Recognition System II block diagram

output when the input voltages are within ±5 percent of each other. During this scan period, each of the two inputs must exceed an adjustable minimum threshold in order to allow the comparator to operate. At the comparator output there is a series of pulses for each 10-ms period only when a symmetrical signal exceeding the scanner thresholds is located with its axis of symmetry at the center of the delay line. These pulses, when averaged, represent a time-varying measure of the degree of symmetry.

A threshold applied to the comparator output can be made to operate at a predetermined level of symmetry for all signals. It is evident that with a typical satellite signal the measure of symmetry would pass through a sharp maximum since the axis of symmetry coincides with the center of the delay line. This suggests that the center of the signal can be accurately determined by differentiation, thereby defining the point where the slope of the signal waveform reverses sign. The "slope reversal" will always occur 1 second (one-half of the length of the delay line) after its occurrence in real time regardless of the length of the signal, even if it extends out to 10 seconds. When the decision threshold is applied to the slope-reversal output instead of the undifferentiated comparator output, a further benefit is possible since some nonsatellite signals may possess considerable symmetry but will not follow the rapid slope-reversal characteristic of all satellite responses.

The symmetry decision is rendered as a normalized pulse or contact closure for a nominal period of 150 milliseconds.

SYSTEM DESIGN

The completed Symmetry Recognition System II was assembled in one standard rack cabinet, as shown in Fig. 6(a). At the top of the cabinet are located the three vacuum-tube power supplies providing +150 volts, +100 volts, and -150 volts. Next, the monitor oscilloscope and its input control panel below provide rapid access to the primary waveforms to facilitate checking adjustments and other operating conditions. The delay line control chassis carries the amplifiers, multivibrators, and logic for the insertion and readout of signals stored in the delay line. It is followed by the process control chassis containing the input dc level corrector, event detector, and symmetry measuring and decision circuits. The next five chassis contain the Beam-X (BX) magnetic beam counters and the scanner diode matrix which time all readin-readout functions associated with the operation of the delay line. The large chassis at the bottom contains the signal insertion relays and their associated driver logic, the capacitors constituting the delay line stores, and the associated readout cathode followers. A rear view of this cabinet is shown in Fig. 6(b), where the preamplifier and the relay drive logic matrix are located along with the remaining power supplies.

Figure 7 shows some of the construction techniques employed in the Symmetry Recognition System II. Typical of the process and delay line control chassis is the "card" mounting shown in detail in Fig. 7(a). Each circuit is mounted on a prepunched terminal board, which in turn is supported on an aluminum plate. Active heat-producing transistors and vacuum tubes are fastened directly to the plate, which serves as a heat sink and affords shielding when mounted adjacent to other similar circuitry. Folded tabs on each end of the plate support a connector plug and provide a withdrawal handle. Thirteen assembled plates or cards can be inserted in a 3-1/2-in. standard rack width chassis containing matching slide-in channels. The chassis provides electrical and thermal paths for shielding and heat removal. Adequate space is available for components and wiring external to the circuit cards. Figure 7(b) shows two examples of subminiature vacuum tube circuits, while Fig. 7(c) demonstrates the application of Nuvistor triodes and a Nuvistor tetrode to high-gain dc amplifier circuits. Mercury-wetted relays have also been card-mounted in two forms, shown in Fig. 7(d).

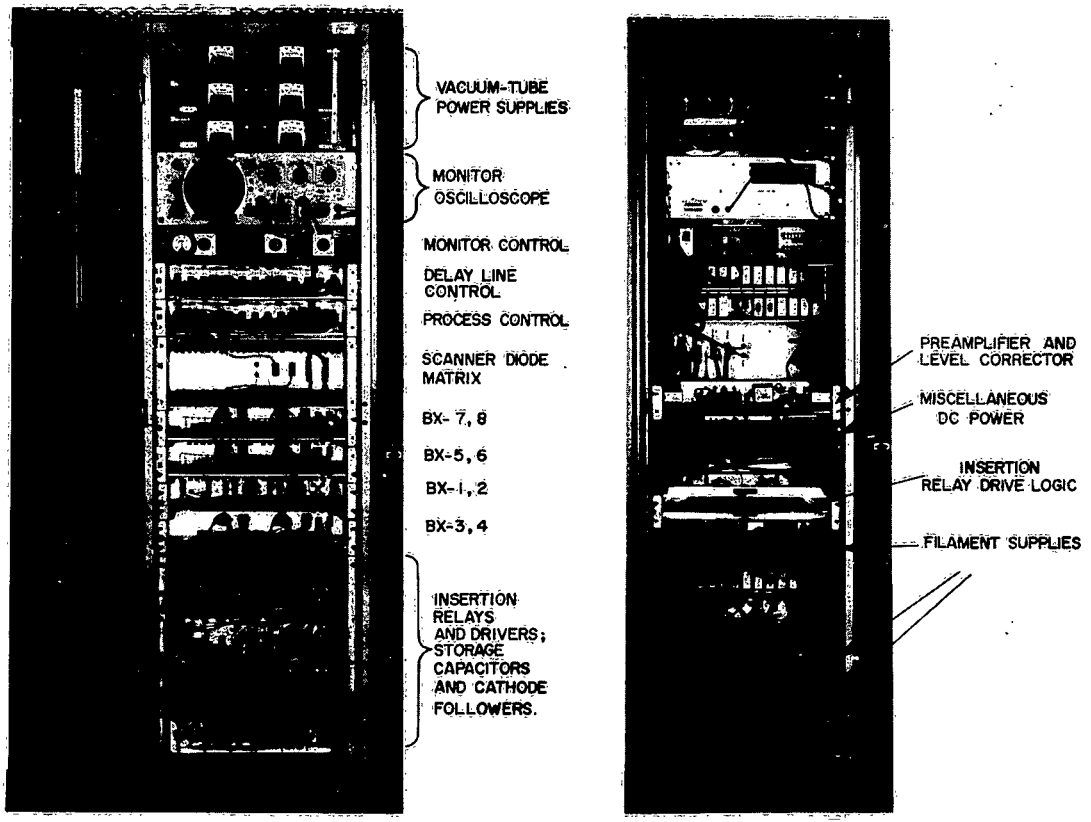
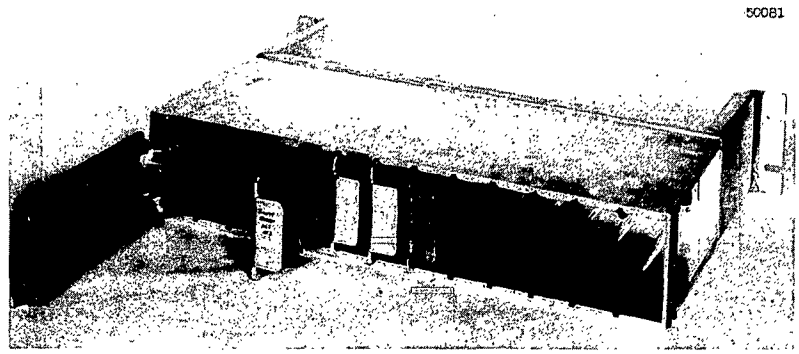
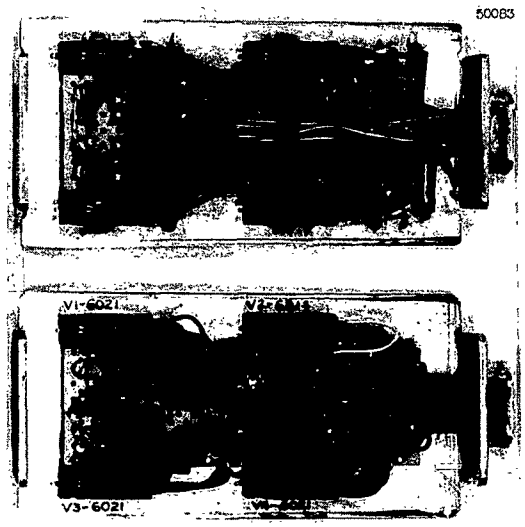


Fig. 6 - Symmetry Recognition System II equipment: (a) front view, (b) rear view

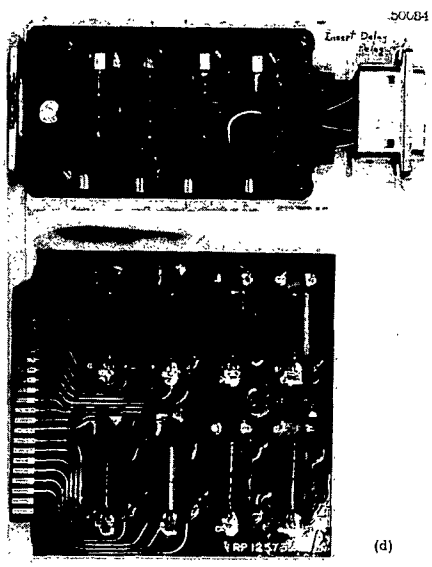


(a)



(b)

(c)



(d)

Fig. 7 - Some construction details of the rack-mounted Symmetry Recognition System II: (a) chassis construction showing circuit plug-in cards. An extension card permits servicing a circuit card while in use; (b) circuit card construction details showing four capacitor store cathode-followers above, and the inhibit and insert units for the 99-count and 101-count logic below; (c) circuit card construction details showing the Insertion Driver unit below, and the Comparator unit above. Both triode and tetrode Nuvistor tubes are used in the high-performance operational amplifiers; and (d) mercury-wetted relay card assemblies for store cathode-follower input-output control and for insertion delay.

AGC SIGNAL SOURCE

The completion of the pattern recognition equipments was scheduled for about the time of the SPASUR comb-filter system installation, thereby affording no opportunity to observe the range of signal characteristics of the latter during the design period of the former.

A review of the SPASUR comb-filter design showed it to be composed of eleven narrow-band intermediate-frequency amplifiers, each driving a group of narrower bandwidth contiguous filters. A total of 161 filters of this type divide the 16-kc bandwidth of each baseline receiving system into slots only 100 cps wide prior to detection. Although each slot or comb "tooth" is followed by a detector and further postdetection filtering, the development of 161 agc networks was considered unnecessary. Accordingly, agc was developed and applied in each of the eleven preceding group i-f amplifiers. Each of the eleven agc's thus developed control the signal level for seven to sixteen filter "teeth."

As a result of this review, it was agreed that eleven emitter-followers would be installed by the contractor to provide group-agc outputs for pattern recognition. The signal levels would be about -0.5 volt maximum riding on a -4.0 volt bias. Signal-to-noise ratio computations indicated the group agc signal would be 12 to 13 db poorer than the corresponding individual comb tooth at the output of its postdetection 10-cps filter. In spite of this pessimistic outlook, some hope was held in the fact that the comb-filter system was to be set to respond with an alert signal only when the signal-to-noise ratio exceeded 12 db.

A group agc selector shown in Fig. 8, was designed to select a single agc output when it rose above the common threshold levels of its neighbors. The signal first must be amplified by a factor of 10 and then biased so as to be referenced to ground in order to meet the level requirements of the pattern recognition inputs. It was determined that 6-v gating pulses, designating the narrowband filter group responsible for an alert pulse, were to be available from the Automatic Digital Data Assembler System (ADDAS). Provisions were included to allow one of eleven such pulses to gate "on" a single amplifier, thus excluding any of the noise contributions from the other ten agc's. If these gating pulses are not available, the diode summing network included in the group agc selector will always select the largest amplitude signal.

The need for low-drift-rate, dc, operational amplifiers led to the choice of Philbrick P-2 solid-state amplifiers, which are chopper-stabilized. An output amplifier provides a low-impedance source and may be connected for either signal polarity. Controls include individual group gain and bias settings as well as selected output gain and bias adjustments.

INPUT AND DELAY LINE

Delay Line Switching

The control of the delay line proper is accomplished by four decade counters, labeled BX-1 through BX-4, which are driven by a 5-kc clock. These counters drive the signal inserting relays through a set of transistor buffers and a diode logic network, as shown functionally in Fig. 5. The block diagram of the delay line control counters is shown in Fig. 9. Each BX counter is driven by a flip-flop, which in turn is driven by the preceding decade counter, or by the clock (Fig. 10) in the case of BX-1. BX-1, BX-2, BX-3, and BX-4 are the basic delay line control counters. BX-1 and BX-2 divide the clock pulse repetition rate by 100 in order to provide the pulse rate to BX-3 and BX-4, which control the switching of the signal into the delay line. If the unit was to be a delay line without a scanning function between signal insertions, BX-1 and BX-2 would not be required, and the clock could be run at 50 pps. Since the delay line is scanned once in both directions

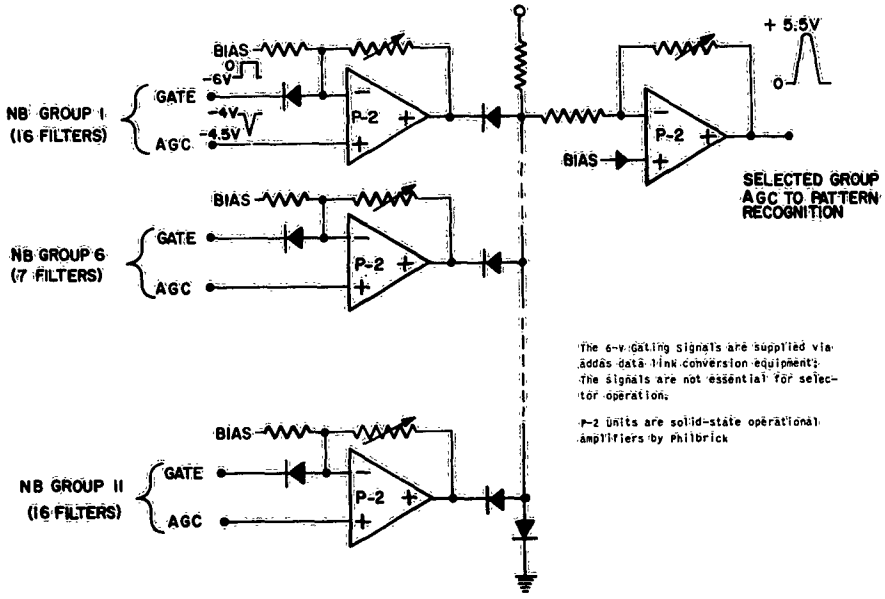


Fig. 8 - Group agc selector block diagram

during each insertion time increment, BX-5 and BX-6, and BX-7 and BX-8 are required to perform the scanning switching function. Because each storage element holds the signal sample for the full time of the delay (2 seconds), the starting point of the scanners must be rotated at the same rate as the point of signal insertion. This is accomplished by removing one pulse from each 100 to the BX-5 and BX-6 counters and by adding one pulse to each 100 to the BX-7 and BX-8 counters (see Figs. 9 and 11). This has the effect of causing the starting point for the scanner counters to advance "clockwise" with respect to the delay stores one step for each signal insertion period of 20 millisecond. The inhibiting of one pulse for each scan by BX-5 and BX-6 is accomplished by setting the inhibit flip-flop with a pulse from amplifier T_8^1 - T_9^2 (the superscript gives the BX number and the subscript gives the target number on that BX counter). The flip-flop inhibits each 100th pulse from the clock to BX-5 and BX-6. The delayed pulse T_9^2 resets the flip-flop in order to release the inhibit. The delayed T_9^2 pulse is gated through to BX-7. This pulse, which is delayed for a period of 10 μs so that the counter will properly count the extra pulse, causes BX-7 to receive one extra count per scan. The net effect is that when the BX-5 and BX-6 counters are logically connected to scan backwards through the delay line stores, and BX-7 and BX-8 are logically connected to scan forward through the delay line stores, their starting point advances forward through the stores one step each scan. Details on this sequencing and the scanner logic are given in the section "Inhibit and/or Insertion Waveforms."

Decade Counters

The wiring schematic of one of the eight counters is shown in Fig. 12. The decade counter tube V1 is a magnetic beam switching tube of the BX-1000 (6710) type (see Burroughs Beam-X brochures BX-535 and 535A). The counter is made to advance by triggering the flip-flop consisting of tubes V2 and V3. The plates of the flip-flop are coupled to the BX-1000 even and odd grids through cr differentiating networks, thus causing these BX-1000 grids to be driven alternately by negative pulses. When a particular target is

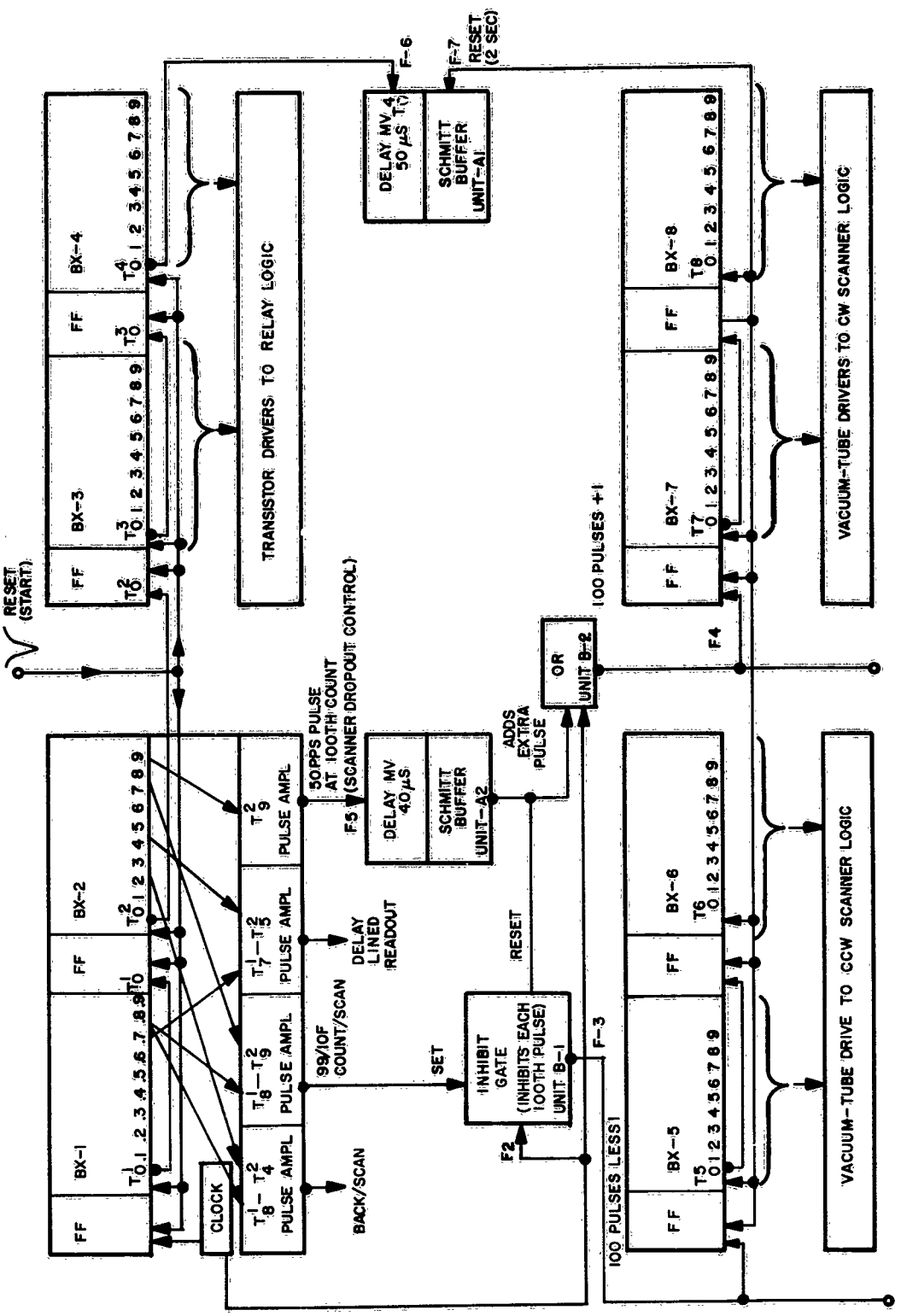
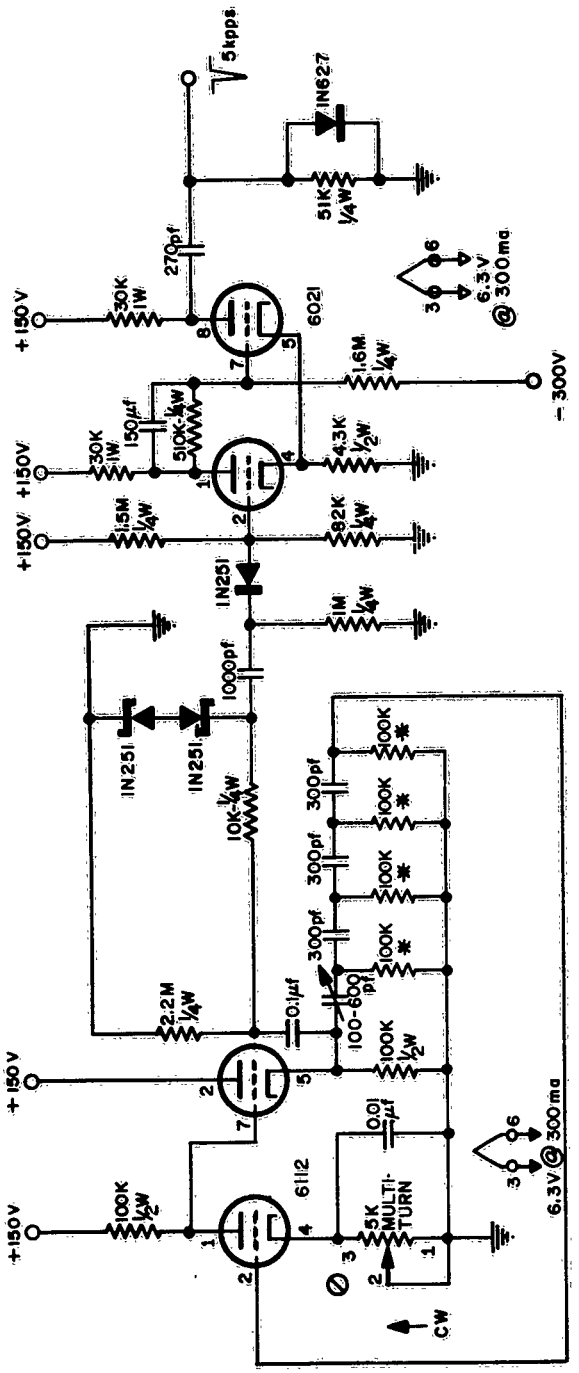


Fig. 9 - Counting and scanning logic circuit



* METALLIZED-TYPE RESISTORS

Fig. 10 - 5-kc clock pulse oscillator located in the BX-1 - BX-2 chassis

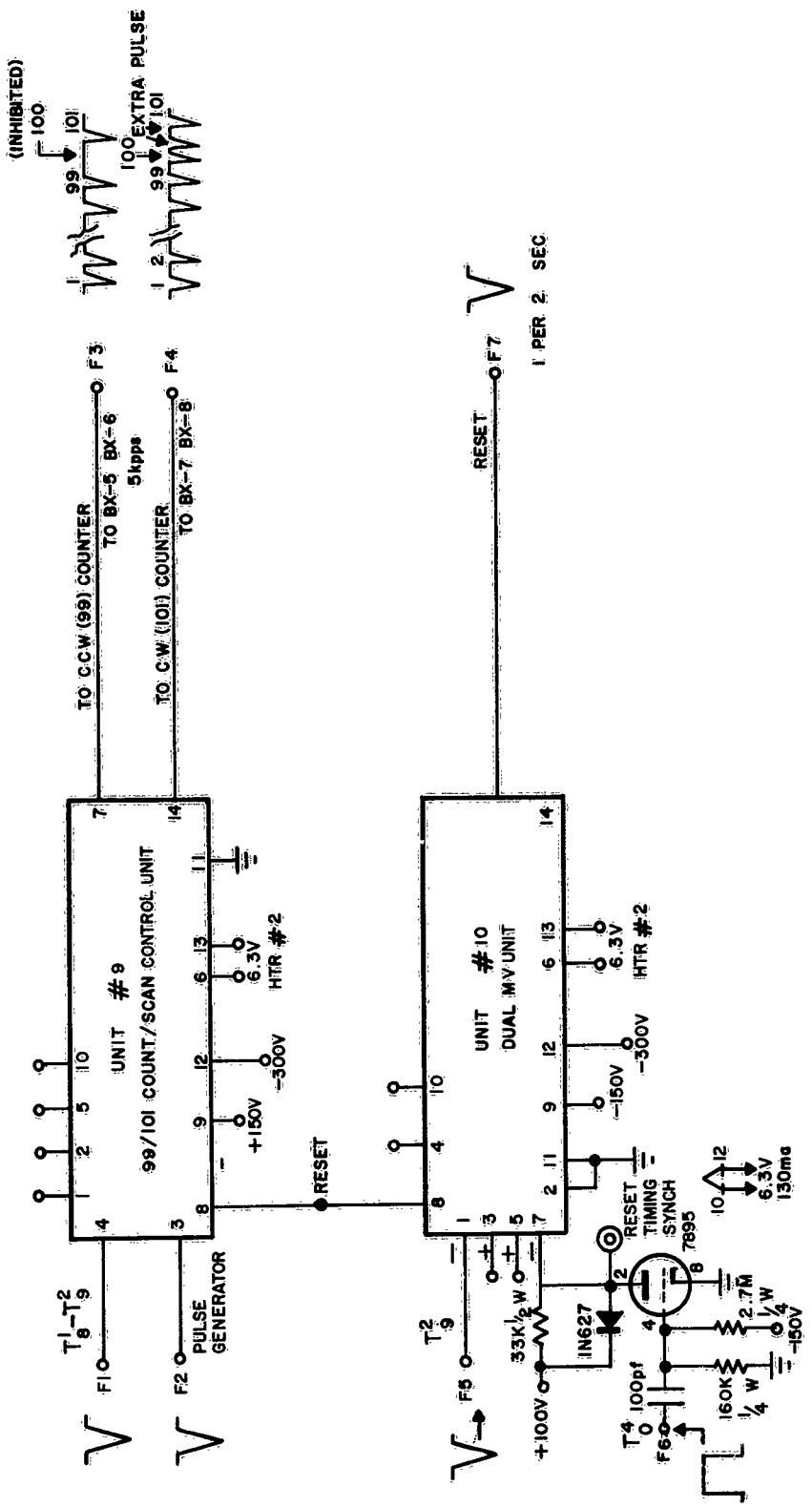


Fig. 11 - Counter control section

conducting, say T_o, and the even grids are driven by the negative pulse from the flip-flop, T_o is cut off and T_1 then conducts. When the odd grids are then driven by a negative pulse, T_1 cuts off and T_2 conducts. This process continues as long as the flip-flop is triggered. When T_9 cuts off, T_0 conducts and the switching tube repeats the cycle. In the case of operation with the delay line, methods of automatically starting and resetting the magnetic beam switching tubes are necessary. The magnetic beam switching tube conduction has to be started by lowering the voltage on the spade voltage associated with the selected starting target. In this case, the selected target is the zero (T_0) target. The starting feature is accomplished by V5 in Fig. 12. When the power is applied to the BX-1000, no target is conducting, allowing the cathode of V5 to be at a low potential. V5 conducts and causes the zero spade (S_0) voltage to be lowered, causing the zero target (T_0) to conduct. When the target starts conducting, the cathode of V5 is raised and V5 is cut off. A lead from the plate of V5 also couples to the driving flip-flop such that the flip-flop is set to the correct condition for causing the BX-1000 to advance when the next input pulse is applied to the flip-flop. The tube V4 is used for resetting the counters and for maintaining the synchronization of the scanner counters BX-5, BX-6, BX-7, and BX-8. Reset is accomplished by cutting V4 off with the reset pulse from BX-4 through the corresponding delay MV (Figs. 9 and 11). When V4 cuts off, the BX-1000 is cut off. The action of V5, described above, restarts the counter at the correct position. In this manner, the scanners are resynchronized each 2 seconds, and the system automatically starts itself when the power is turned on.

Pulse Amplifiers

The wiring schematics of the pulse amplifiers in Fig. 9 are shown in Fig. 13. The tubes are normally cut off, and the output is an amplified pulse formed from the logic network at each input to the pulse amplifiers. In each case, the output pulse corresponds to the instant when a counter target is going from the conducting state to the nonconducting state. For example, the T_9^2 pulse occurs when target 9 of BX-2 cuts off. The control pulses from the other three pulse amplifiers are formed by the logic network gating one target signal from the unit counter (the higher speed counter) by another signal from the ten counter (see Fig. 9). For example, the 99/101 count per scan pulse is formed from the cutting off of target 8 on BX-1 (T_8^1) after being gated by target 9 on BX-2 (T_9^2). This corresponds to the extra pulse position in the delay line scanners. The other control pulses are formed in a similar manner.

Diode Logic Matrix and Input Buffers

The diode logic network and the transistor input buffers for analog signal insertion into the delay line are shown in Fig. 14. The buffers are NPN transistors whose bases are connected to the BX counter targets through 47-K resistors. Only one target on each counter is conducting, and the transistors connected to these conducting targets are cut off. The transistor collectors drive the diode logic network, which is set up in the form of a matrix. As the BX-3 and BX-4 counters advance through their count, the buffers are connected to the diode matrix such that the outputs of the matrix advance sequentially 00 through 99, as shown in Fig. 14. The outputs of the matrix are normally low (approximately -6.8 volts) except at one point which corresponds to the logical "and" of the nonconducting buffers. This point is high (approximately zero volts) and drives the transistor (D_j^i), which energizes the selected delay line relay driver transistor (R_{ij}), as shown in Fig. 15. When the transistor (R_{ij}) conducts, the corresponding relay is energized. All of the relay drive transistor emitters are connected to a common line which in turn connects to ground through an inhibit transistor (Inh-1), which is normally conducting. This transistor's base is driven by the inserting transistor (Inh-2) such that Inh-1 cuts off all the relay drive transistors for 2 milliseconds after a step advance in the delay line control.

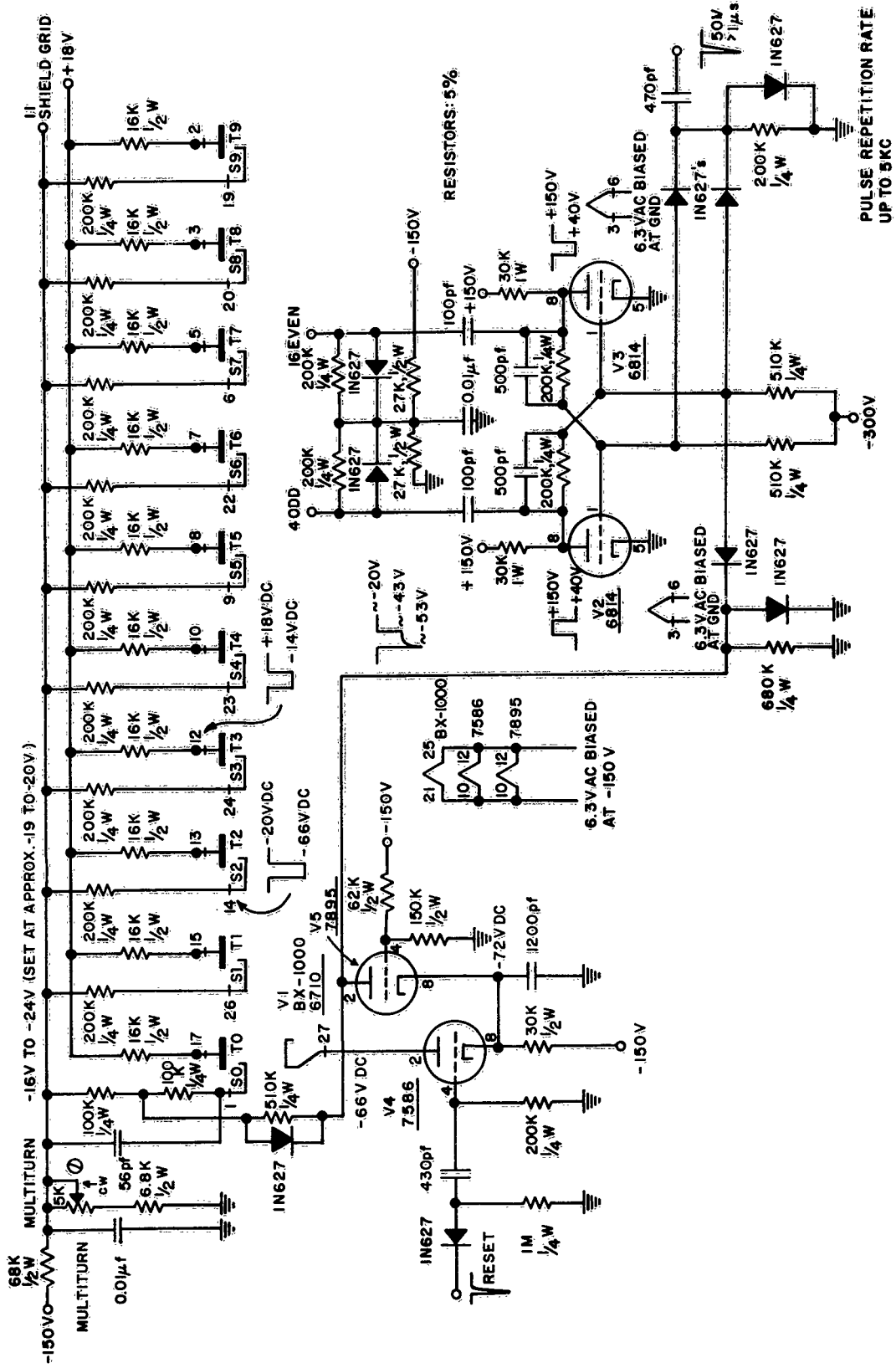


Fig. 12 - Magnetic beam counter

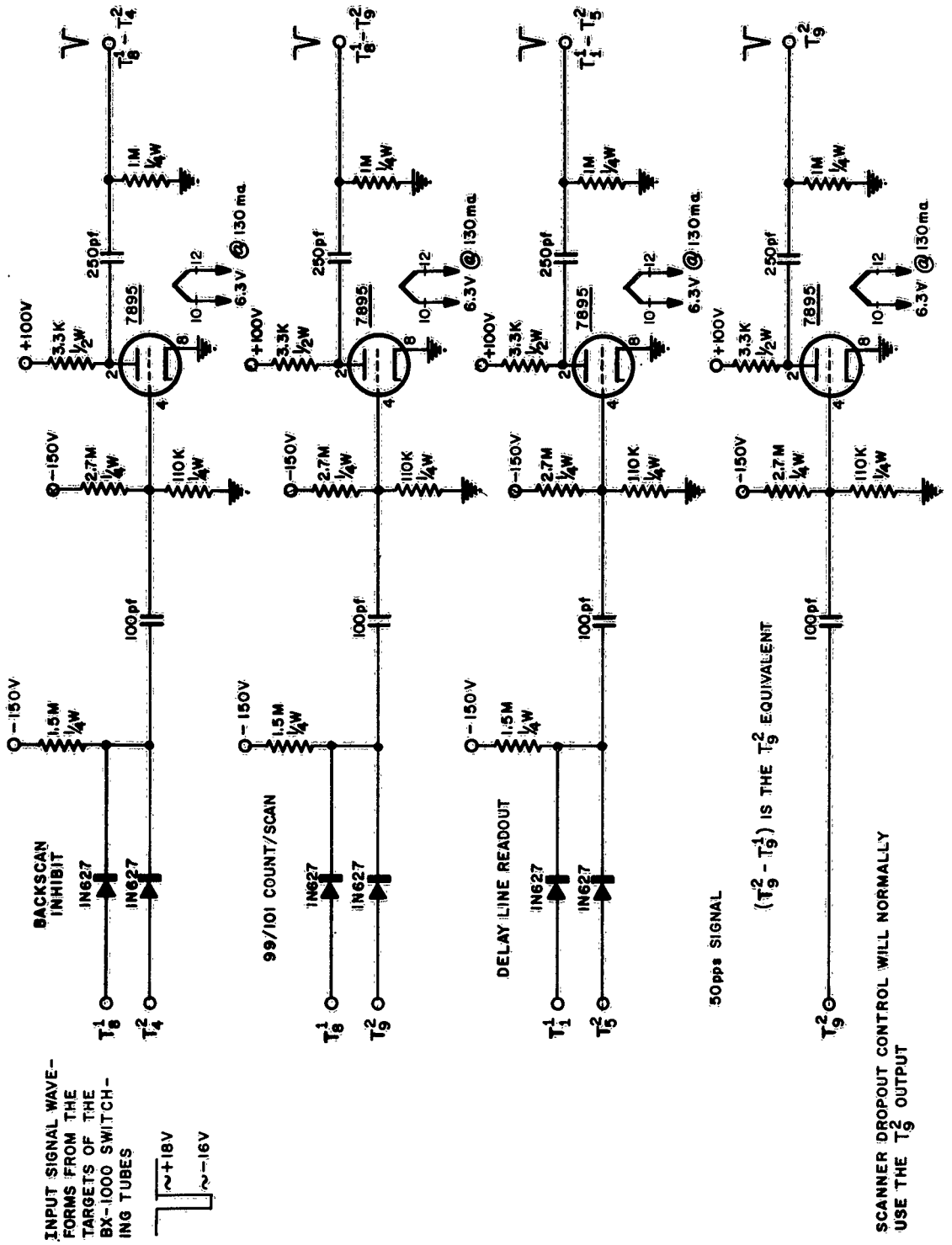


Fig. 13 - Pulse amplifiers (these circuits are located on the BX-1 - BX-2 chassis)

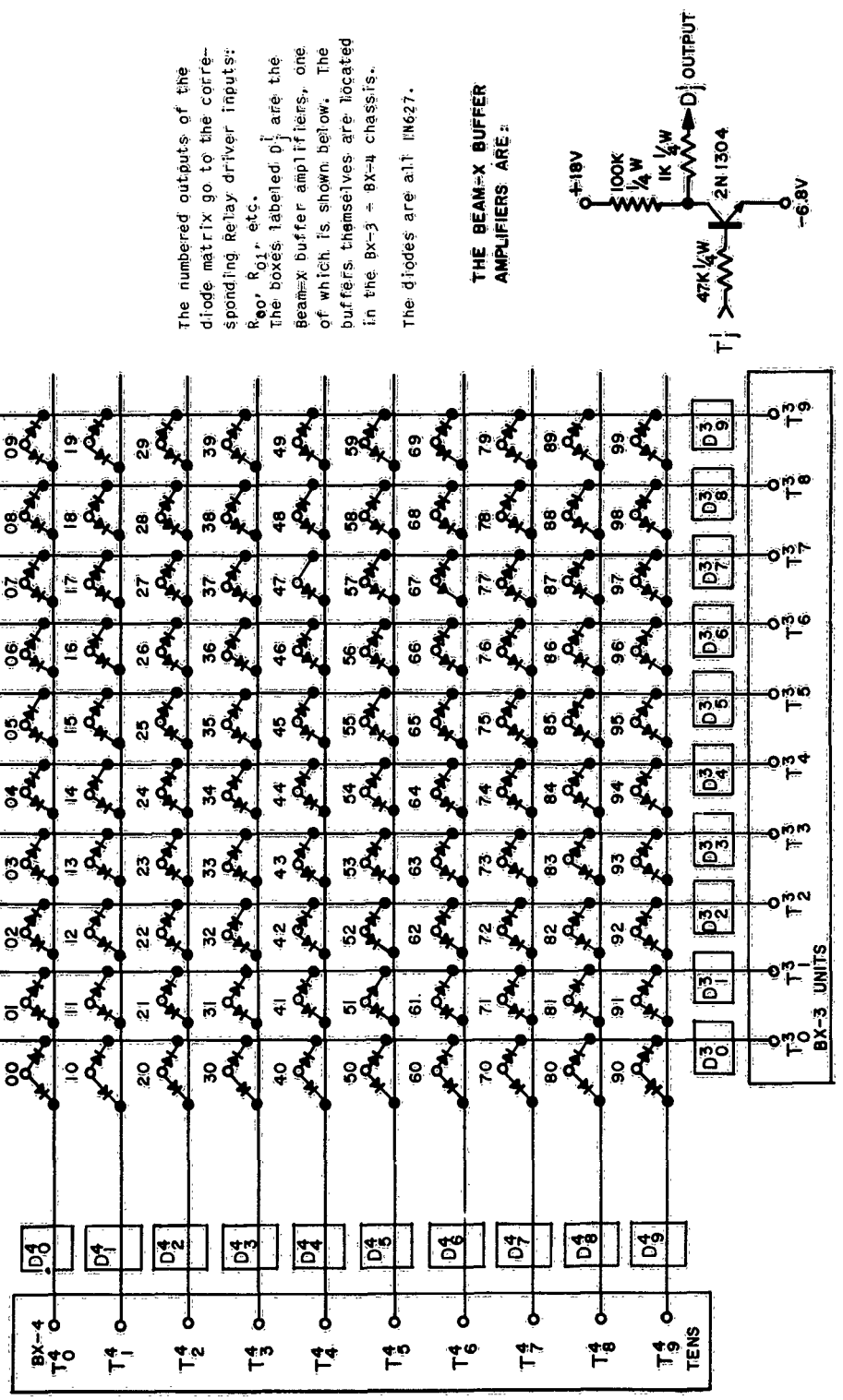


Fig. 14 - Relay drive logic matrix circuit

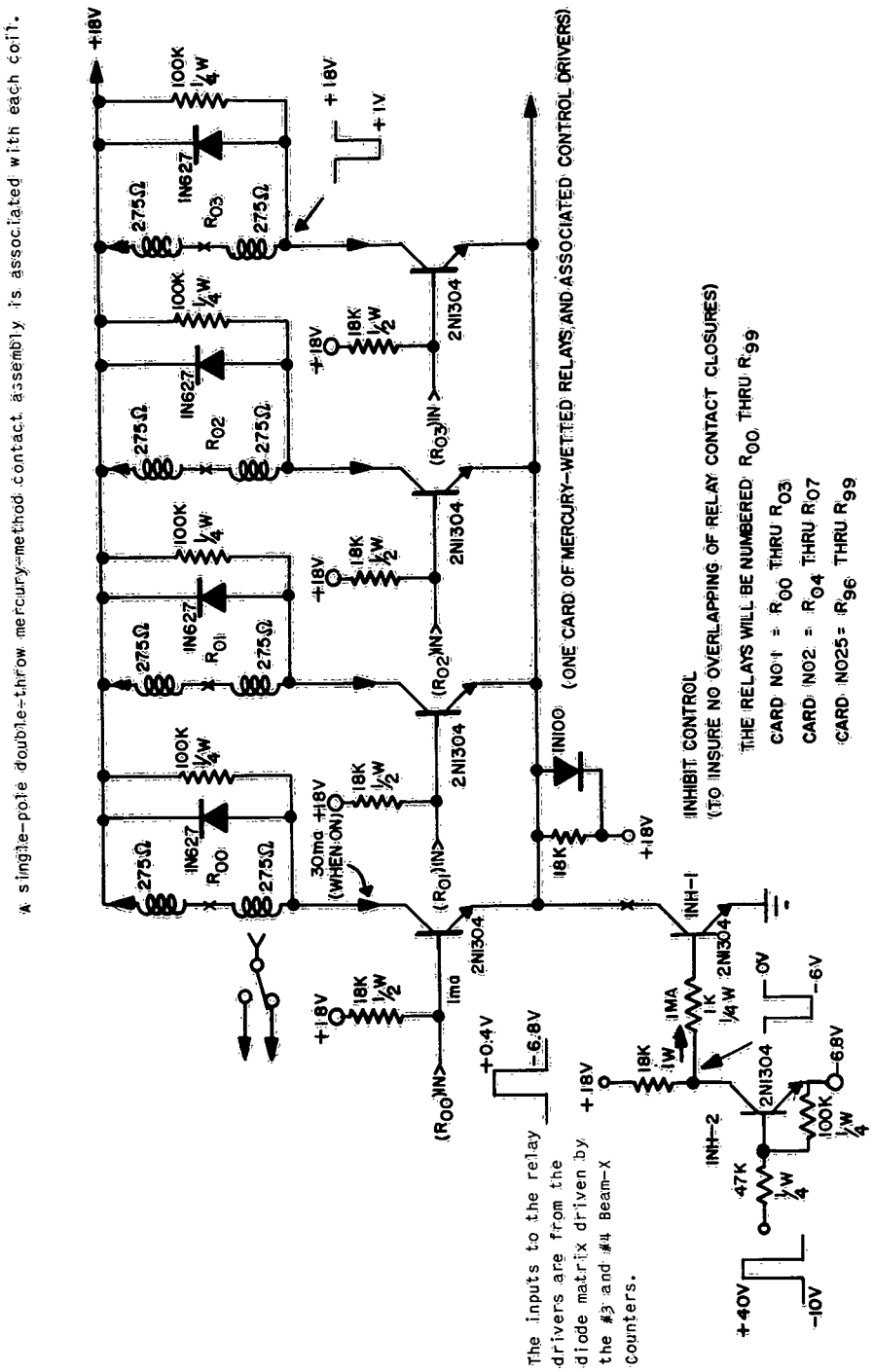


Fig. 15 - Store control relay card assembly and drive circuits

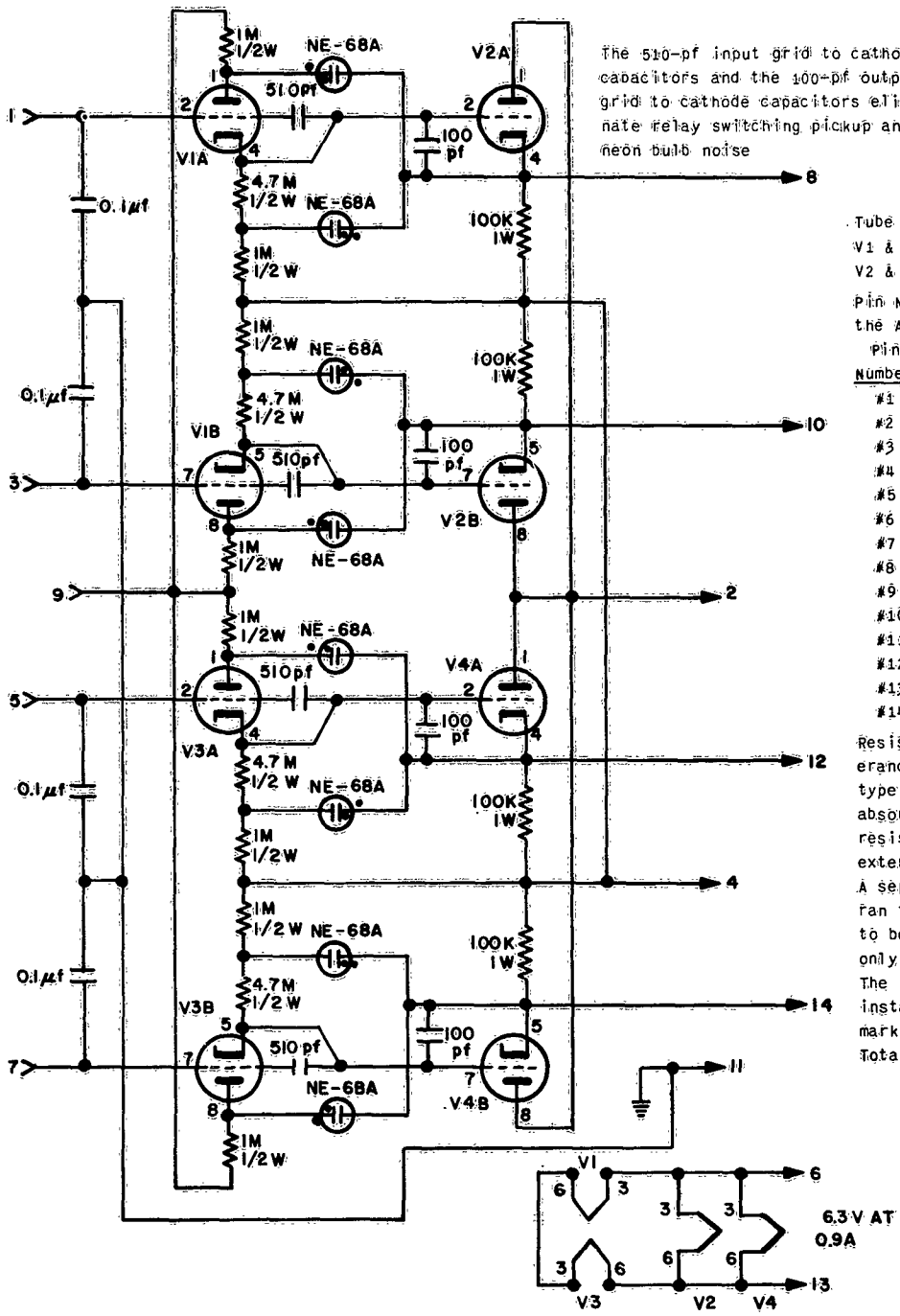
This control pulse comes from the insertion delay MV, which is described later. The purpose of the 2-ms inhibit (Inh-2) of the relays is to insure the opening of the mercury-wetted relay contacts before the next relay in the control sequence is energized. This prevents shorting between storage capacitors during the transition period when the delay line advances one step. In the actual construction, four double-pole relays were mounted on one card, as indicated in Fig. 15 and the lower unit in Fig. 7(d). The storage cathode-followers were also mounted four to a unit, as shown in the wiring schematic in Fig. 16 and at the top in Fig. 7(b). The storage cathode-followers use 6111 tubes at the input and are operated at one-half heater voltage. The input section of each cathode follower is then bootstrapped through the interconnecting NE-68A neon bulbs from the output cathode follower in order to keep the input section in the very low grid current region of operation (2). The grid current of these readout cathode followers is less than 10^{-11} amperes and, consequently, have negligible effect on the accuracy of the stored value during the 2-sec storage period.

SIGNAL INSERTION

The input circuits to the delay line and the delay line circuits are shown in Fig. 5. The normal agc signal is amplified, and the input drifts are removed by the dc level corrector and stabilized dc amplifier. The drift corrector uses two low-noise solid-state Philbrick type P-2 operational amplifiers, as shown in Fig. 17. Additional gain is provided by two cascaded dc amplifiers which are chopper stabilized, as shown in Fig. 18. Figure 18(a) shows the interconnections between the dual dc amplifier unit and the dual ac amplifier unit which connect the two units to the stabilized dc amplifier section shown in Fig. 5. The unit shown in Fig. 18(b) consists of a dual dc amplifier unit, and a dual ac amplifier unit is shown in Fig. 18(c). The output of the stabilized amplifier provides the input to the insertion driver.

The insertion driver interconnections with the delay line stores are shown in Fig. 19. The delay line relay contacts at the inputs of the storage capacitors and the outputs of cathode followers are controlled by the delay line counters 1 through 4, as explained under Delay Line Switching. The insertion delay relay contacts in Unit No. 1 in Fig. 19 operate each time one of the delay line store relays operate. The insertion delay relay contacts are timed to close after the selected store relay contacts close and to open before the store relay contacts open. Thus, in the period during which the insertion delay contacts and the selected store contacts are closed, the storage capacitor is charged to a voltage such that the output of the readout cathode follower is made equal to the input signal to the insertion driver. Because the delay line is 2 seconds in length and consists of 100 sections, the cycle time for each store is 20 milliseconds. Because of the operating times of the relays, the insertion delay relay contacts are closed approximately 6 to 12 milliseconds during the middle portion of the 20-ms period. This insures no contact overlap due to relay operate time and the contact bridging common to the mercury-wetted contacts used in the relays. Appendix A gives the analysis of how the various offset voltages and gain errors of the cathode followers are corrected in the actual signal insertion process.

The insertion driver unit circuit is shown in Fig. 20. A single-pole double-throw switch is provided for accepting either a positive or a negative signal. The two inputs are attenuated such that the final inserted signal magnitude is the same regardless of the input polarity chosen. A zero adjustment is provided at the negative input. A positive feedback potentiometer β is provided so that the open loop gain of the overall amplifier can be made large (greater than 5000). The negative feedback loop includes two 100K resistors and, external to points 5 and 8 on Fig. 20, the selected relay, capacitor, and cathode follower. The junction of the two 100K resistors connects to the insertion driver output through two avalanche diodes (1N714) connected back-to-back. These diodes prevent the amplifier from saturating during the switching transition period. (The principle of operation of the insertion driver is given in Appendix A.) The circuit which provides



The 510-pf input grid to cathode capacitors and the 100-pf output grid to cathode capacitors eliminate relay switching pickup and neon bulb noise

Tube Types:
V1 & V3: 6111
V2 & V4: 6021

Pin Numbers refer to those on the Amphenol 57-10140 Plug

Pin Number	Use
#1	#1 input
#2	+100VDC input at 6ma
#3	#2 input
#4	-150VDC input at 6.4ma
#5	#3 input
#6	Htr. input
#7	#4 input
#8	#1 output
#9	+150VDC input at 0.4ma
#10	#2 output
#11	Ground
#12	#3 output
#13	Htr. input
#14	#4 output

Resistors are standard 5% tolerance; capacitors are plastic type with low dielectric absorption and high leakage resistance. Capacitors mounted external to the C.F. Unit.
A separate ground lead is to be ran thru the circuit. Chassis to be grounded at one point only.
The NE-68A neon bulbs to be installed with the polarity mark as indicated.
Total power: 7.3 watts.

Fig. 16 - Capacitor store and cathode-follower wiring for four-store card

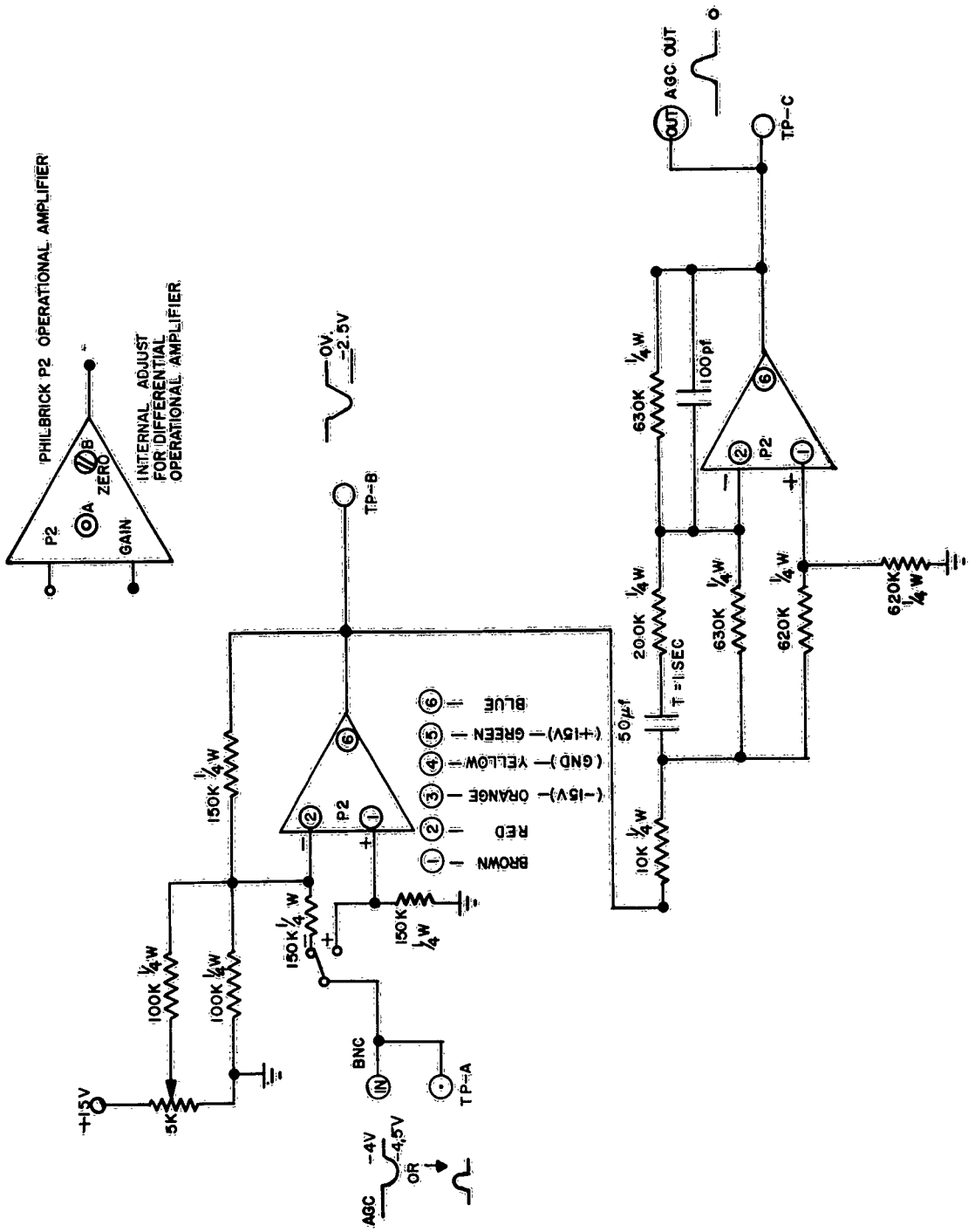


Fig. 17 - Selected group agc preamplifier and drift corrector

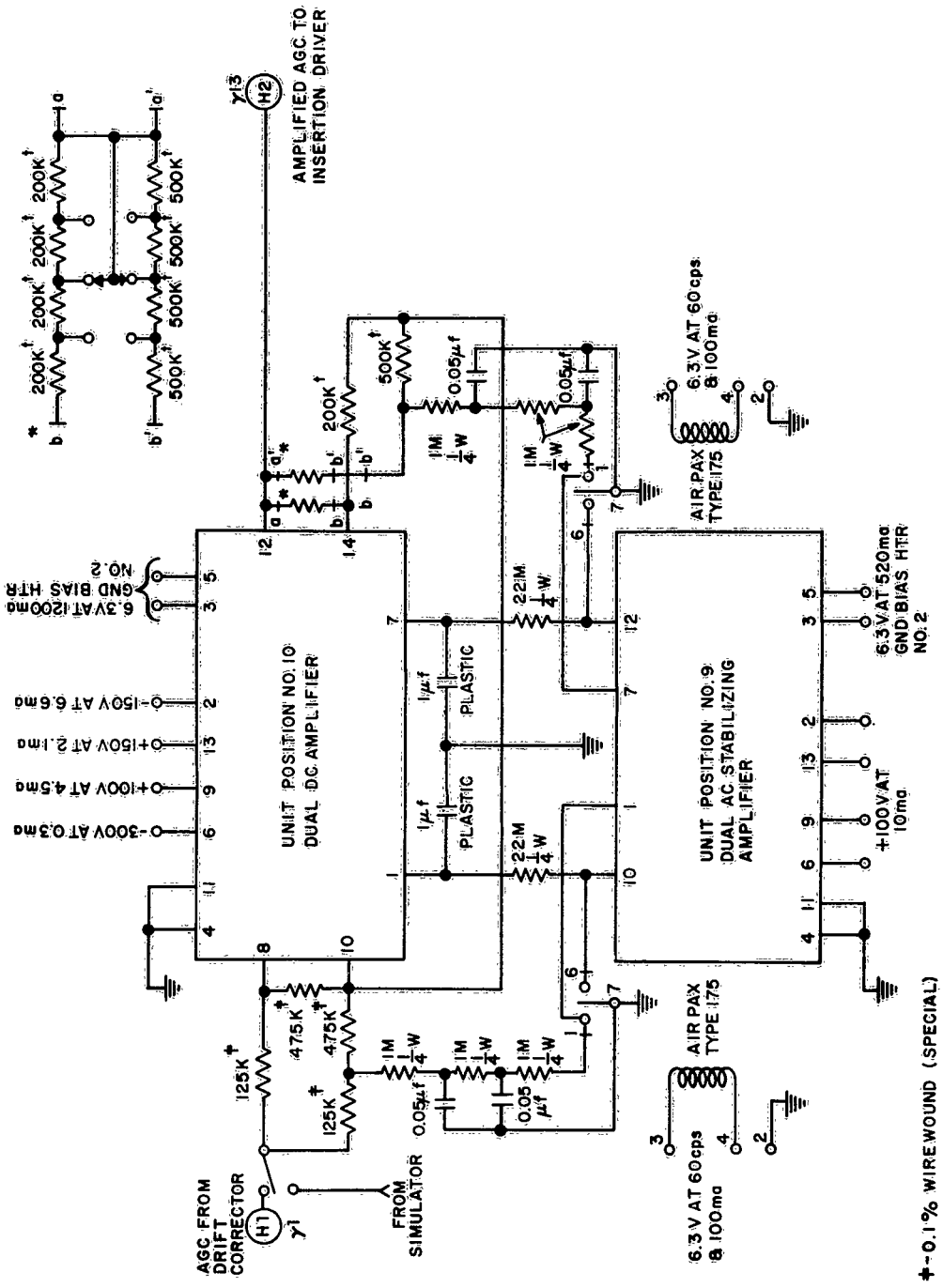


Fig. 18 - Additional gain provided to the drift corrector, shown in Fig. 17, by two chopper-stabilized, cascaded, dc amplifiers. (a) stabilized agc amplifier, (b) dual dc amplifier unit diagram, and (c) dual ac stabilizing amplifier unit diagram.

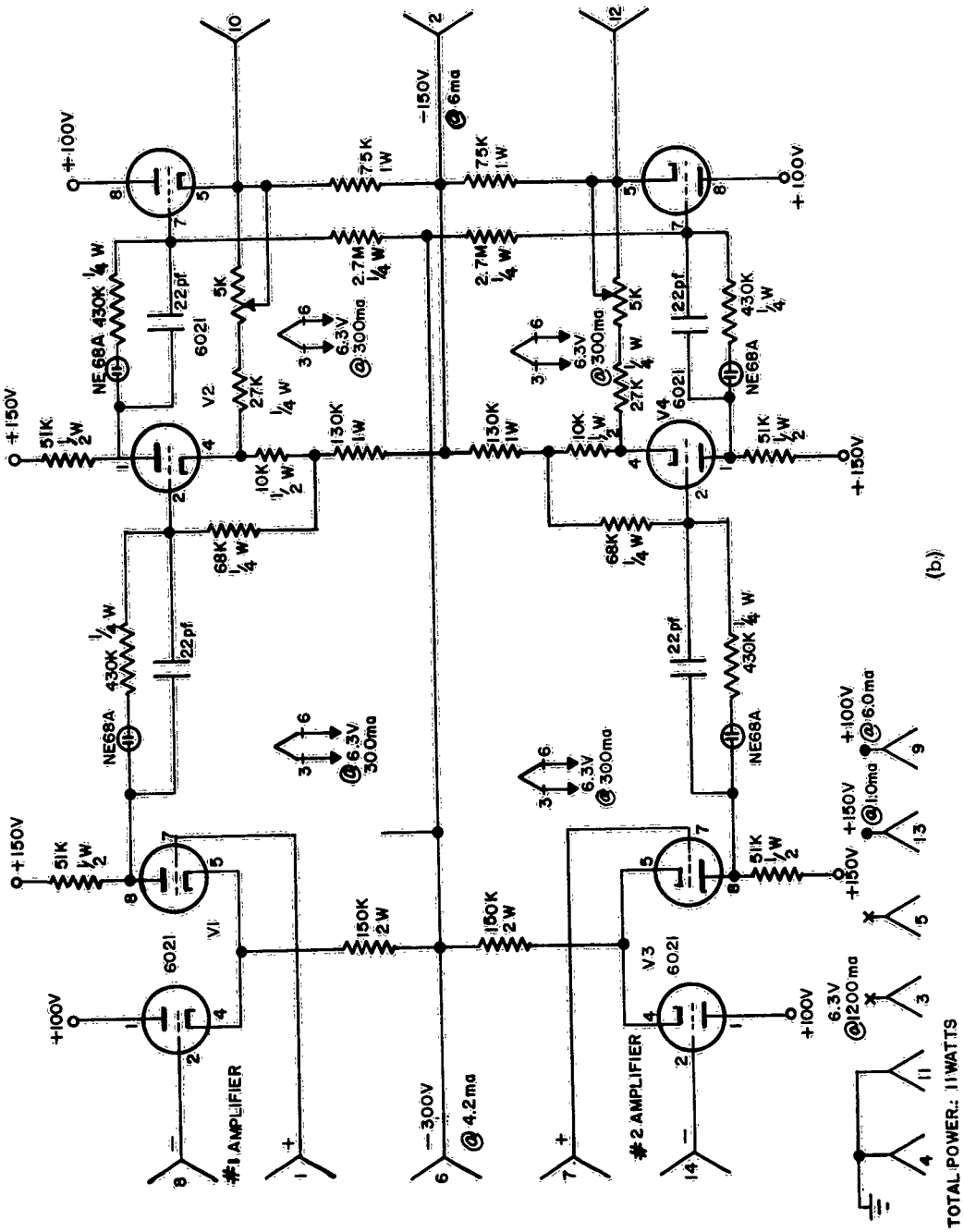


Fig. 18(continued) - Additional gain provided to the drift corrector, shown in Fig. 17, by two chopper-stabilized, cascaded, dc amplifiers. (a) stabilized age amplifier, (b) dual dc amplifier unit diagram, and (c) dual ac stabilizing amplifier unit diagram.

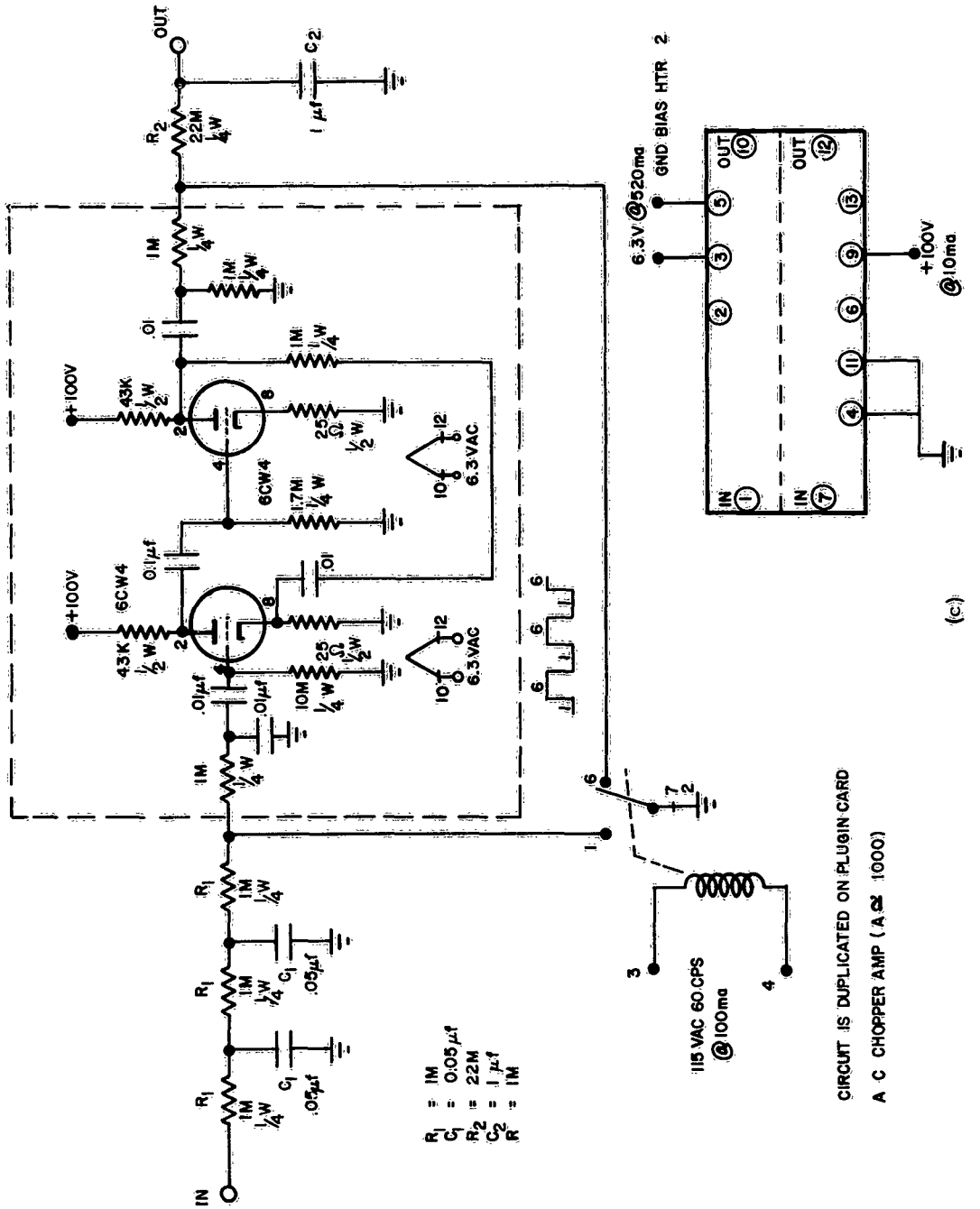


Fig. 18 (continued) - Additional gain provided to the drift corrector, shown in Fig. 17, by two chopper-stabilized, cascaded, dc amplifiers. (a) stabilized agc amplifier, (b) dual dc amplifier unit diagram, and (c) dual ac stabilizing amplifier unit diagram.

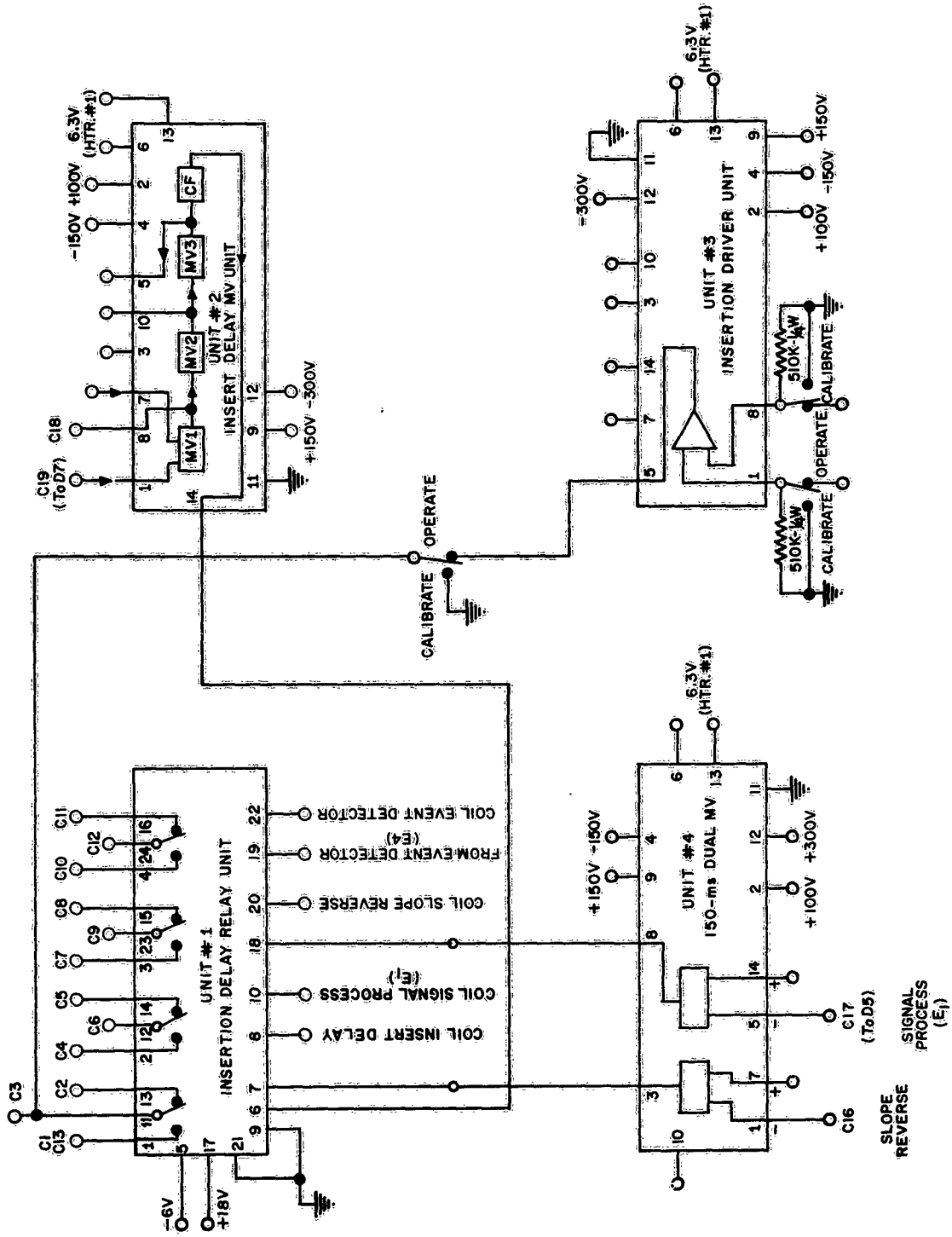


Fig. 19 - Delay line insertion section block diagram

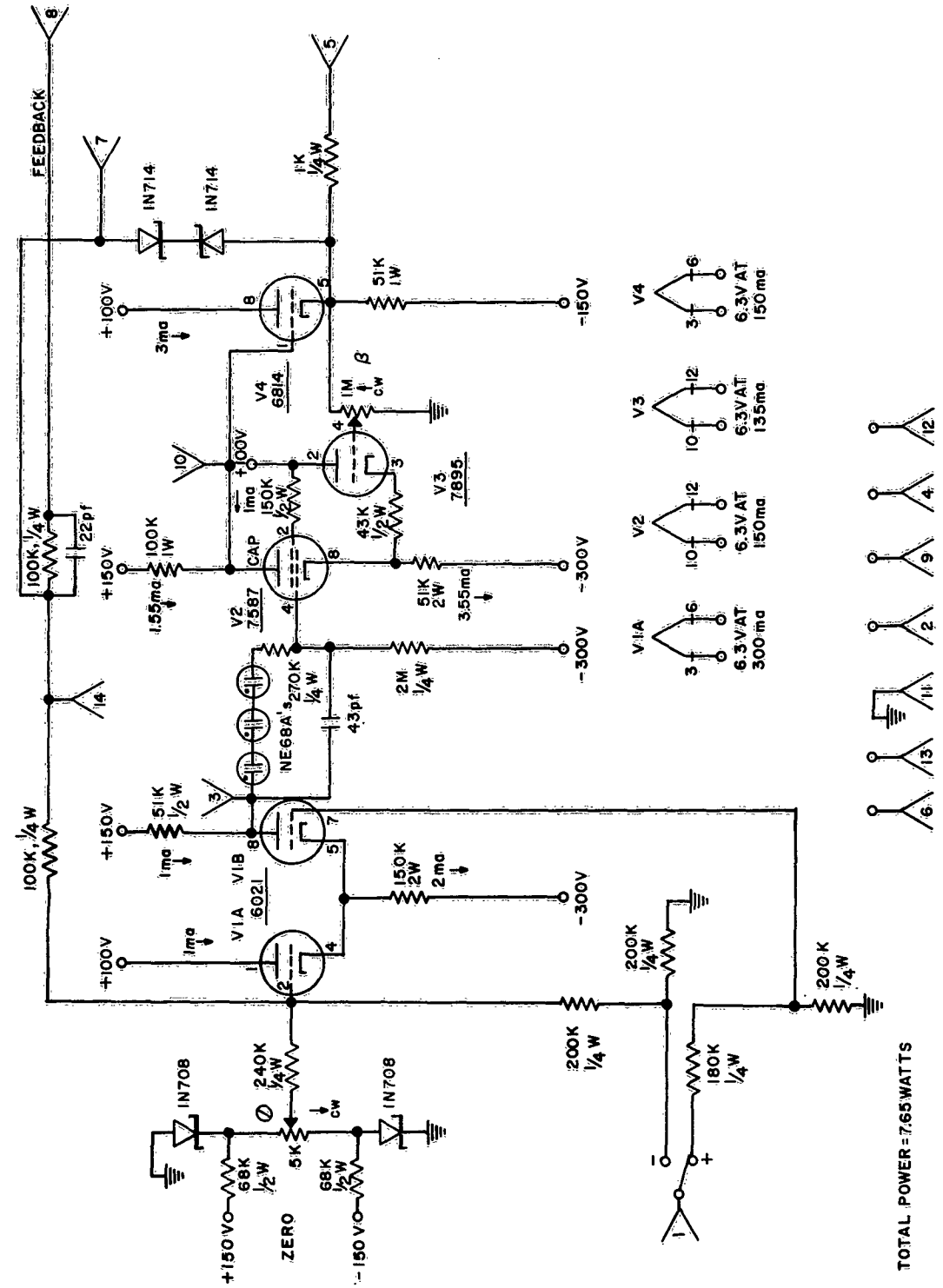


Fig. 20 - Insertion driver circuit

the timing for controlling the insertion delay relay is shown in Fig. 21, and the insertion delay relay circuit is shown in Fig. 22. In Fig. 21, the inhibit multivibrator (MV1) is driven by the output (T_9^2) of the BX-2 counter. MV1 provides a 2-ms pulse (Inh-2) which inhibits the energizing of all of the delay line store relays (Figs. 15 and 19). This allows all of the relay contacts to open before the next delay line store is connected to the insertion driver. MV1 then drives MV2 which provides a 2-ms delay, thus allowing the selected store relay to close before triggering MV3 which then activates the insertion delay transistor relay driving circuit for 6 to 12 milliseconds (Fig. 22). At the end of 20 milliseconds, MV1 is again triggered, and the above is repeated for the next delay line signal insertion.

INHIBIT AND/OR INSERTION WAVEFORMS

The Burroughs beam switching tube counters (BX-5, BX-6 and BX-7, BX-8) which drive the 99 and 101 scanner diode logic circuits are driven by pulses generated by the inhibit and/or insertion plug-in unit of Fig. 23. This unit consists of (a) two Schmitt trigger circuits, each of which is continuously driven by the 5-kc clock pulse generator, (b) a flip-flop inhibit circuit, which is controlled by an external set pulse (T_8^1, T_9^2) from the pulse generator (Figs. 9 and 13), and (c) a 40-μs delayed reset pulse (T_9^2) from MV1 (Fig. 24). The flip-flop inhibits the 100th clock pulse, thus allowing VX-5 and BX-6 to count to 99 during each insertion period. The 40-μs delayed T_9^2 reset pulse, which drives the flip-flop inhibit circuit, also provides an additional pulse to the 101-count Schmitt circuit through a diode OR gate. Therefore, the 99-count counters (BX-5 and BX-6) are retarded a count each cycle, and the 101 count counters (BX-7 and BX-8) are advanced one count each cycle during each signal insertion period. A timing waveform diagram is shown in Fig. 25.

The output waveforms of the counter tubes BX-5, BX-6, BX-7, and BX-8 are buffered and inverted by the scanner gate driving circuits, two of which are shown in Fig. 26, one each for the tens count and the units count. There are ten similar gate driving circuits associated with each of the four counters BX-5, BX-6, BX-7, and BX-8. Each of the gate driving outputs drives ten logic diodes, which form a part of the overall diode logic matrix shown in Fig. 27.

The delay line storage units (Fig. 16) are numbered from double zero (00) through ninety-nine (99). The 99-count matrix is arranged so that the beginning of the scan is at store 49 and decreases numerically through store 00 and stops at store 51. This is shown in the counting matrix for the 99 CCW in Fig. 27. The 101-count matrix is arranged so that the beginning of the scan is at store 50 and advances through store 99 and stops at store 50. The beginning of each succeeding scan is therefore advanced by one store number. This sequence continues until the starting point of both scanners advance through each of the 100 storage elements of the delay line, requiring a total of two seconds. When the starting point of the scanner operation returns to the 00 store, the scanner counters are reset to the initial start position. This insures synchronization of the scanner counters for each two second period.

The detailed counter timing sequence for the counters is shown in Fig. 28. The locations of the inhibit pulse, extra inserted pulse, and the one-per-two-second reset pulse are indicated. The scanner counting matrices shown in Fig. 27 indicate the counter positions at the start of the first scan after each 2-sec reset.

The output of each of the scanner gating drive circuits shown in Fig. 26 connects to ten diodes, which are logically connected to the scanner diode analog gate circuits shown in Fig. 27. The scanner gating drive circuits all normally conduct, except for one in each tens count and one in each units count counters. When the gating drive circuits are conducing, the junction of the diodes in the analog gate is low and the gate is closed (diodes cut off). The diode logic allows only one analog gate to open for each count in the counting sequence of the scan process.

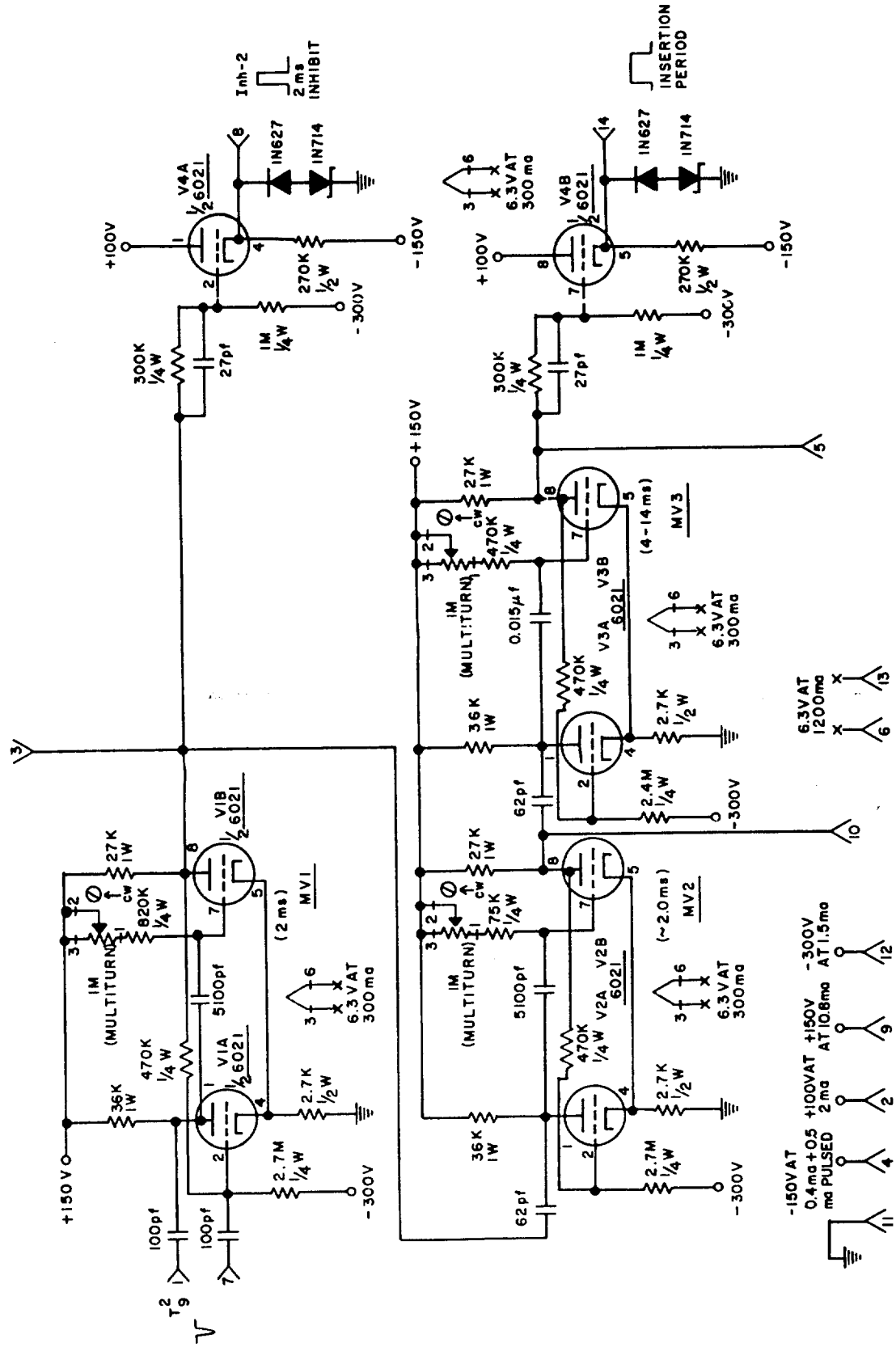


Fig. 21 - Insertion delay circuit

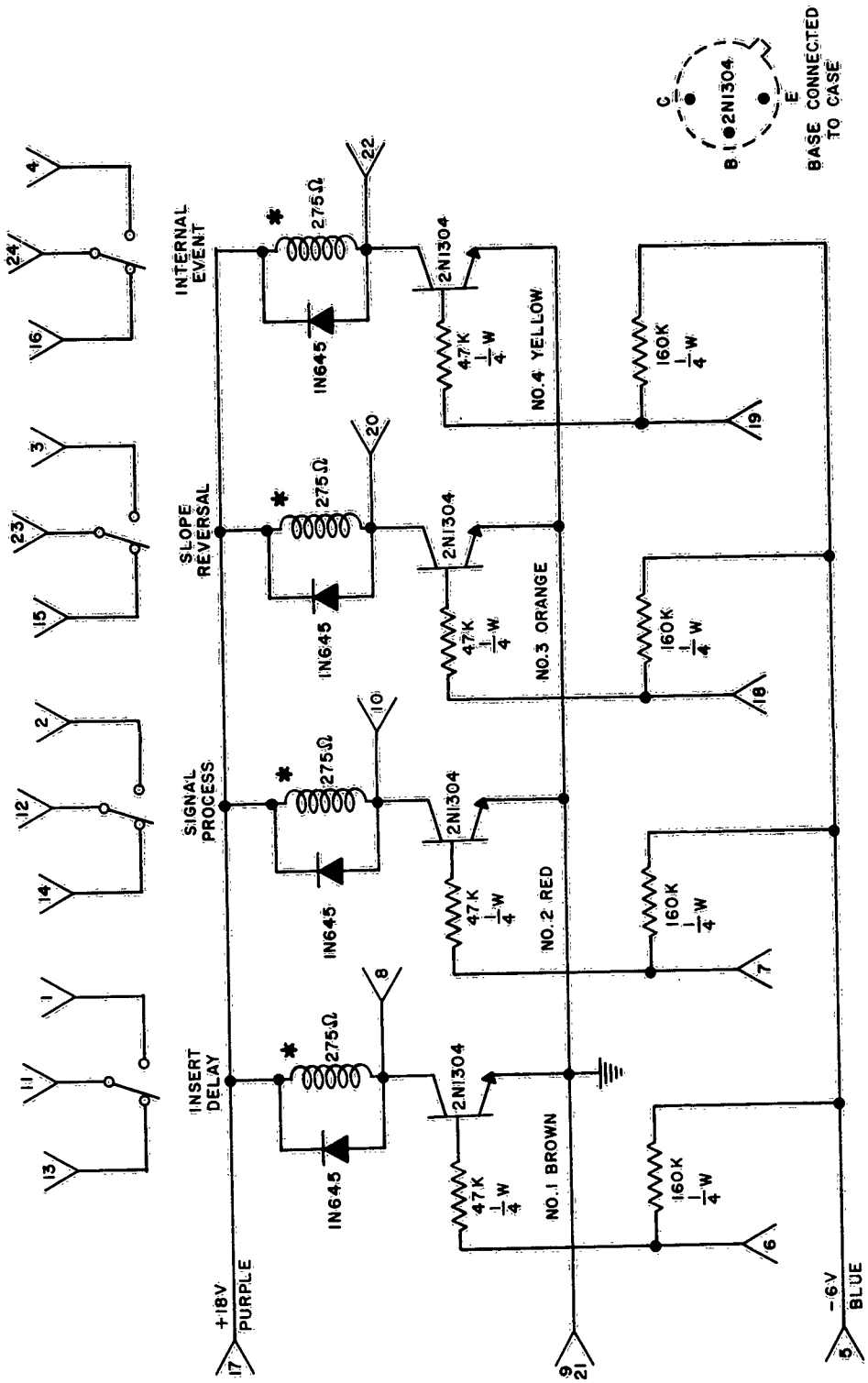


Fig. 22 - Insertion delay relay circuit

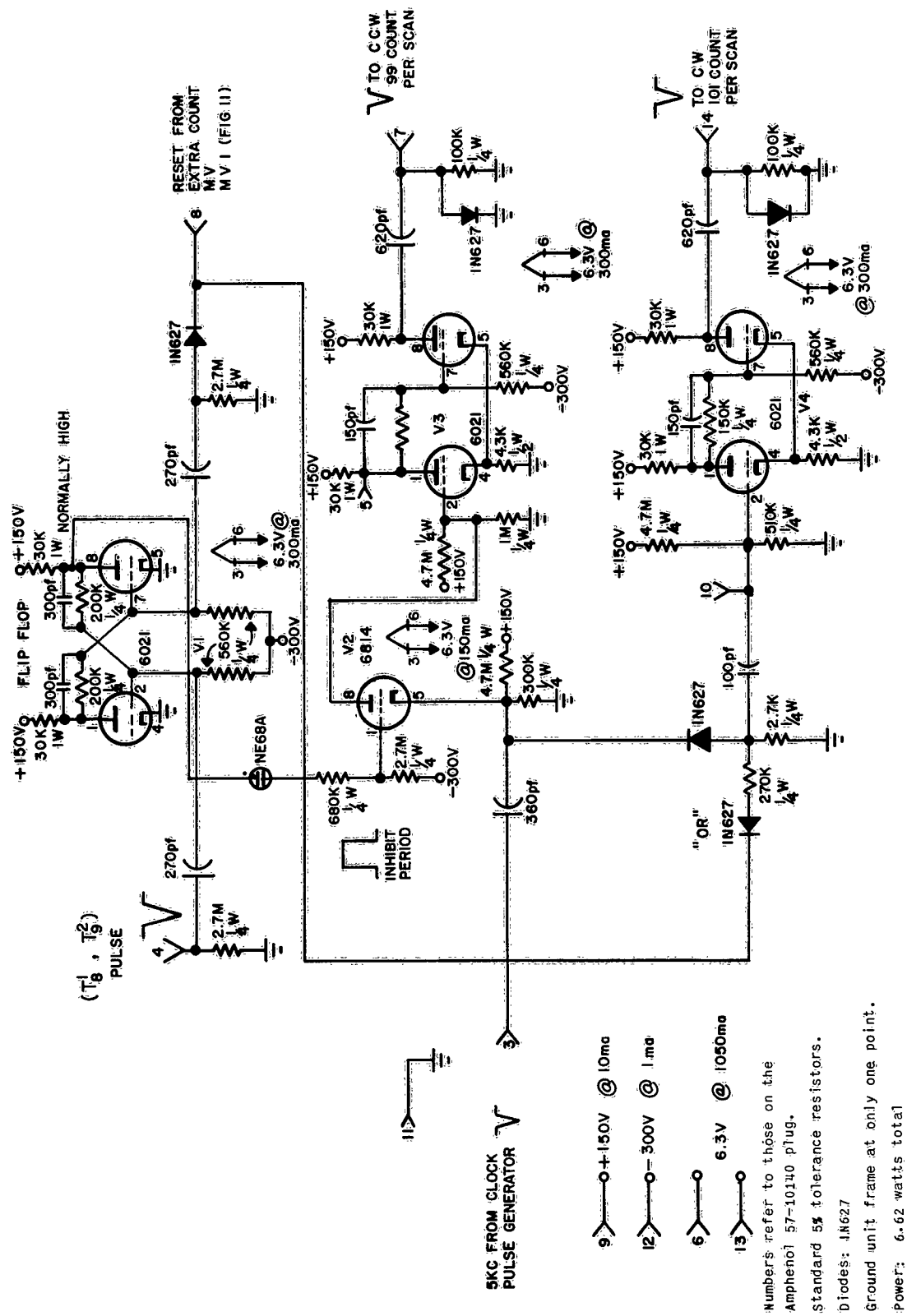
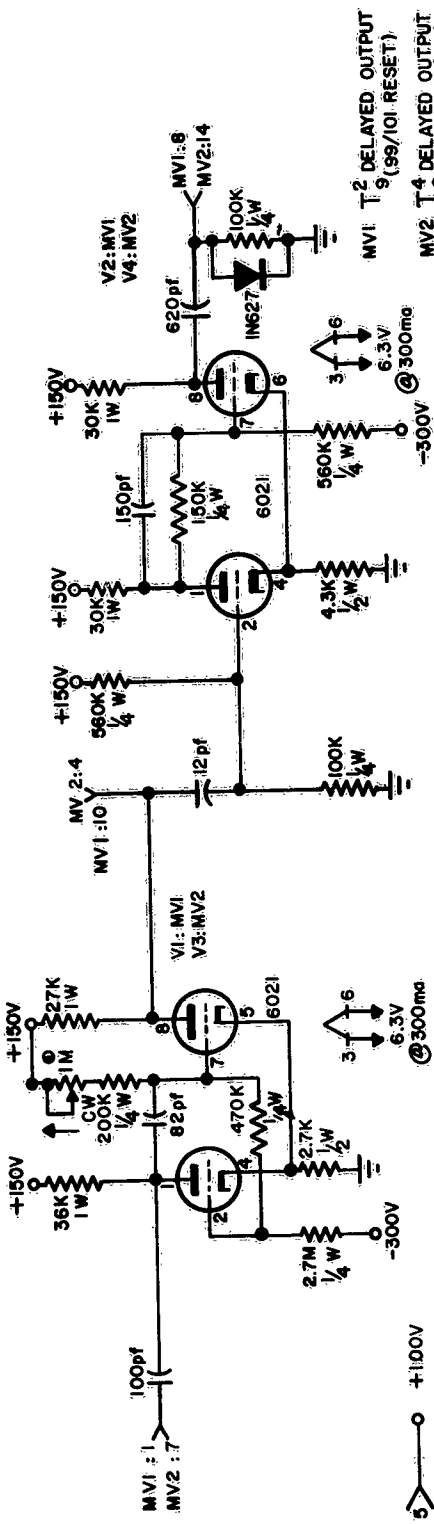


Fig. 23 - Inhibit and insert circuit



Two such multivibrator circuits are on one unit frame. The Amphenol 57-10140 pin numbers are shown for MV1 & MV2. 5% tolerance resistors. Diodes: 1N627

Fig. 24 - Multivibrator circuit

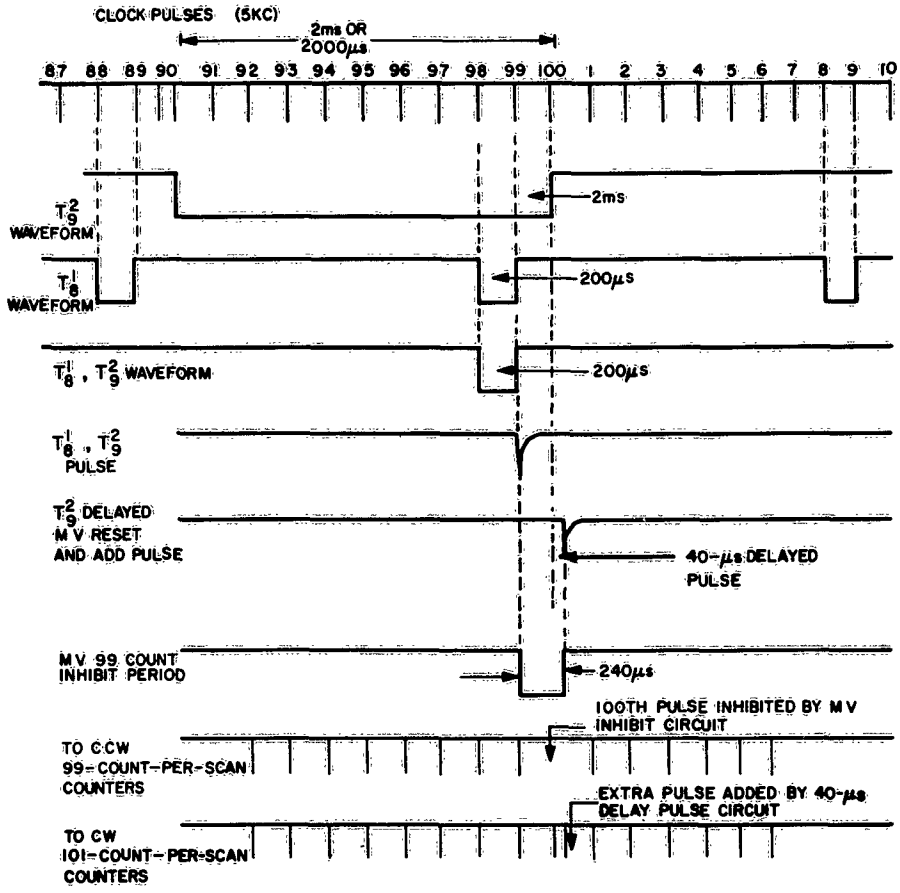
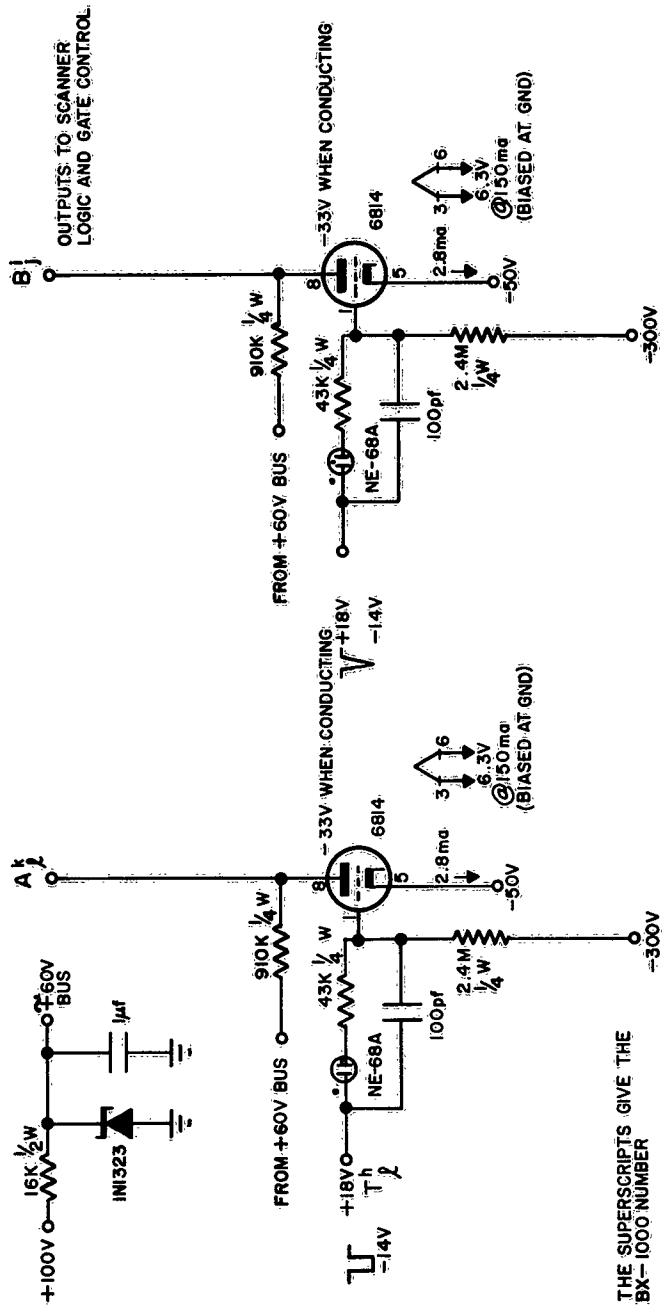
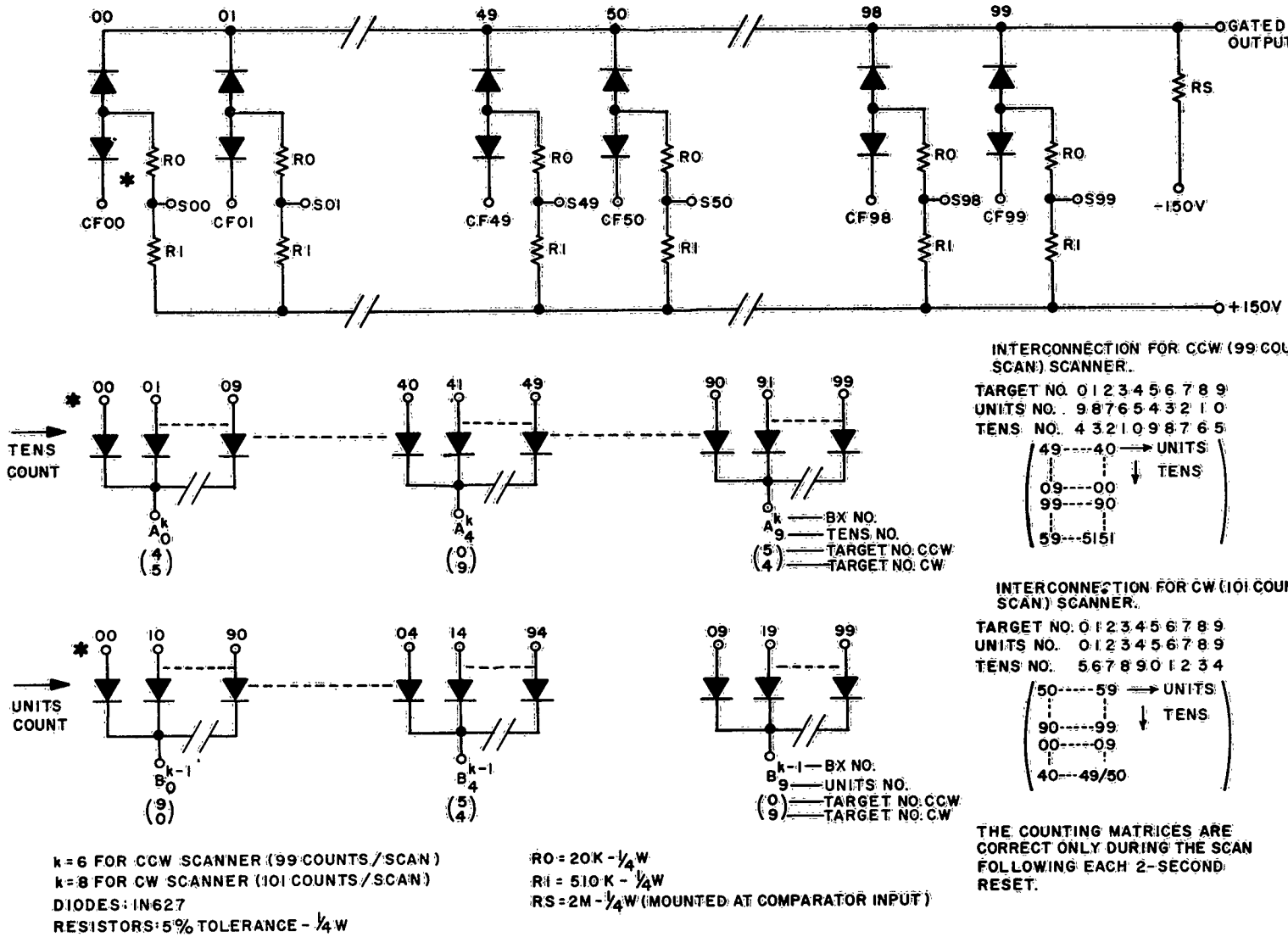


Fig. 25 - Inhibit and insert waveforms



This circuit shows one gate control of ten for the tens count and one of ten for the units count. There will be a total of 40 such circuits associated with BX=5, BX=6, BX=7 and BX=8. Each output shown drives ten logic diodes. (See scanner gating circuit, Fig. 37.) The counter chassis for the CW(10's) and CCW (99) scanners are identical. The controls of the chassis are external, and the logic for proper gating is in the scanner gating chassis. (These circuits are located in the Scanner Counter Chassis.)

Fig. 26 - Scanner gating drive circuit

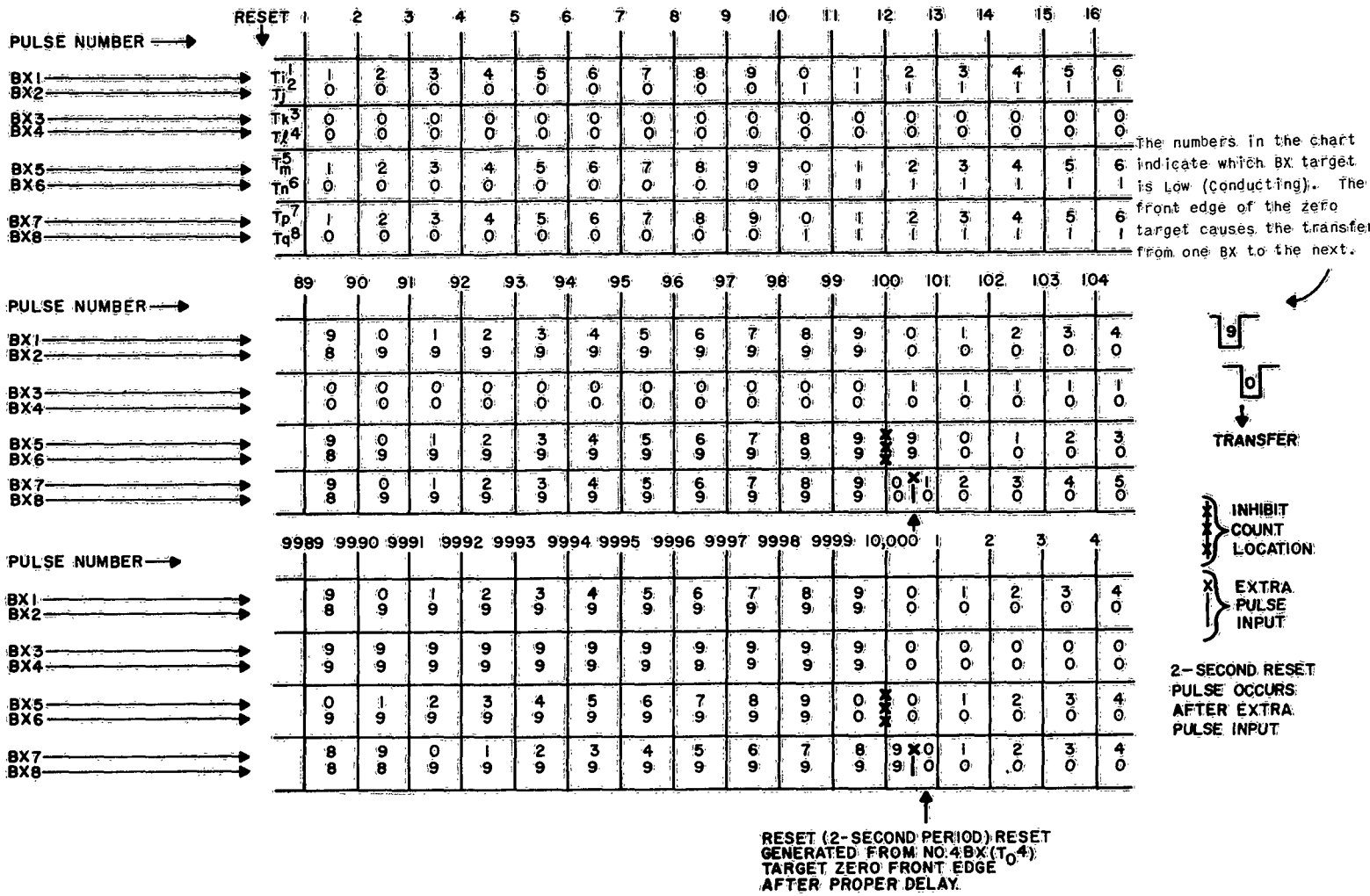


k = 6 FOR CCW SCANNER (99 COUNTS/SCAN)
k = 8 FOR CW SCANNER (101 COUNTS/SCAN)
DIODES: IN627
RESISTORS: 5% TOLERANCE - ¼ W

RO = 20K - ¼ W
RI = 510 K - ¼ W
RS = 2M - ¼ W (MOUNTED AT COMPARATOR INPUT)

THE COUNTING MATRICES ARE CORRECT ONLY DURING THE SCAN FOLLOWING EACH 2-SECOND RESET.

Fig. 27 - Scanner gating and matrix logic circuit



By Definition: All counters are caused to be conducting at the zero target on Reset. The driving Flip-Flops are caused to conduct with the plate driving the even grids to be high on Reset. The first pulse from the clock causes transfer of the first BX from zero target to number one target. Negative Pulse Logic used throughout.

Fig. 28 - Program timing sequence

SIGNAL PROCESSING

Event Detector

Random noise in the agc signal has a degree of symmetry related to the threshold tolerances of the comparator; therefore, a means of limiting some of the nonsatellite comparator responses is necessary. The class of signals of less than 0.2-second duration may be ignored by the symmetry processing section since the SPASUR System geometry precludes satellite responses of this short a duration. These signals are inhibited by the event detector and the T + 1 circuit, indicated in Fig. 5. A more detailed interconnecting operating diagram is shown in Fig. 29. The event detector uses a dual dc amplifier unit (see Fig. 18(b)) and an RC time delay circuit. The agc signal is applied to the point labeled E3, the input to the first dc amplifier which is connected to form a Schmitt-type circuit with very small hysteresis. This is accomplished by using a pair of series-connected avalanche diodes with their cathodes joined, forming the first amplifier feedback loop. When the signal goes above the threshold determined by the voltage at E6, the amplifier output which was high (+30 volts) now goes low (-30 volts), being limited in either case by the breakdown of one of the avalanche diodes. The transition from high state to low state is relatively fast, being on the order of 50 microseconds. The output returns to the high state when the input signal goes below threshold. The output of this first dc amplifier, which is now a threshold detector, cuts off the 7586 vacuum tube which is shunting the 1-μf capacitor. When this tube is cut off sufficiently long (0.2 second in this case), the voltage across the capacitor becomes sufficiently high to trigger a second threshold detector similar to the one described above. This second threshold detector's output is normally low (-30 volts) and goes high (+30 volts) when its threshold, as determined by the voltage at E5, is exceeded. Two single-pole double-throw switches are provided at the input to this second threshold detector. For the operation described above, these switches would be in the internal and negative-polarity positions. When used externally, the second threshold detector can be made to go high from an external event detector, and the polarity switch accommodates either polarity of external input. The output of the second threshold detector (E4) drives a relay circuit (Fig. 19), which provides a switch closure for external event indication from the Symmetry Recognition System.

Because the delay line is two seconds in length, a means must be provided to allow the event-causing signal to advance to the center of the line before the comparator is inhibited. If a signal is shorter than 2 seconds, the event detector output (either external or internal) will end before the center of the signal reaches the center of the delay line. By adding a circuit which provides an output which persists for one second after the end of the event, the above difficulty is overcome. The T+1 circuit indicated in Fig. 29, and schematically in Fig. 30, takes the event detector output and stretches it for one second. A second input is provided to the T+1 circuit from the scanner threshold detector (to be described later). A pair of single-pole double-throw switches is provided to operate the T+1 from the event detector and/or from the scanner threshold detector. The output of the T+1 circuit goes to the "AND" circuit indicated in Fig. 5, and shown schematically in Fig. 31, for use in inhibiting the scanner output comparator circuit. The T+1 circuit consists of two RC charging circuits which drive a diode "AND" circuit (see Fig. 30). When the output of the "AND" circuit goes low (due to the presence of two high inputs to the T+1 circuit), the Schmitt circuit provides an output which goes low (from +30 volts to -70 volts). The proper dc levels at the T+1 output are provided by the constant voltage NE-68A bulbs.

Comparator and Slope Reversal Processing

The scanner output signals, as indicated in Fig. 5, are applied to the two lines designated D1 and D2 in Fig. 31. The terminating 2-M resistors for the scanner diode gates connect to the -150-v supply. These two lines, D1 and D2, are the inputs to the comparator unit and to the logical "AND" circuit for the scanner threshold detector.

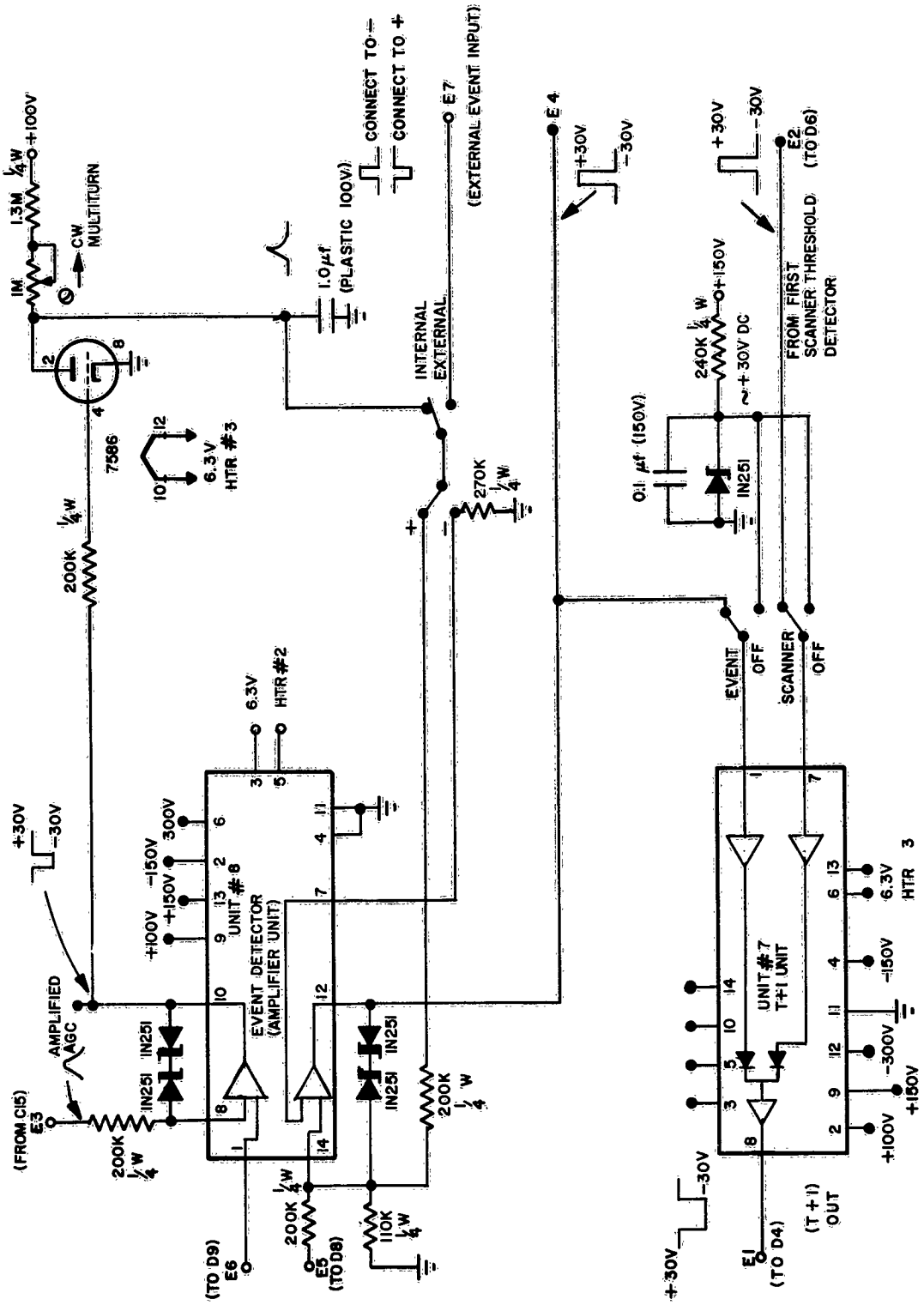
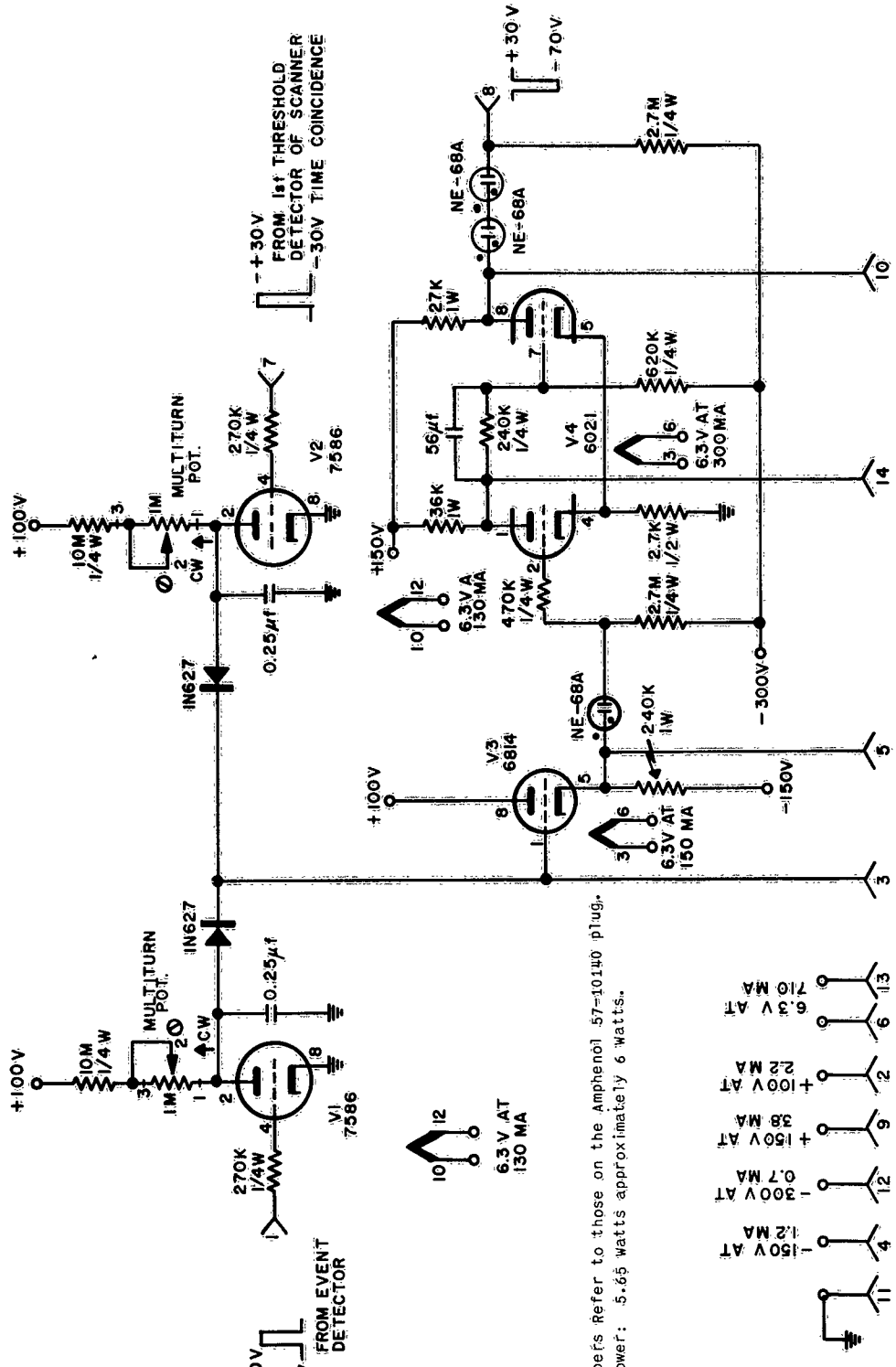


Fig. 29 - Event detector and T+1 section circuit



Pin Numbers Refer to those on the Amphenol 57-10140 plug.
Total Power: 5.65 watts approximately 6 watts.

Fig. 30 - T+I unit

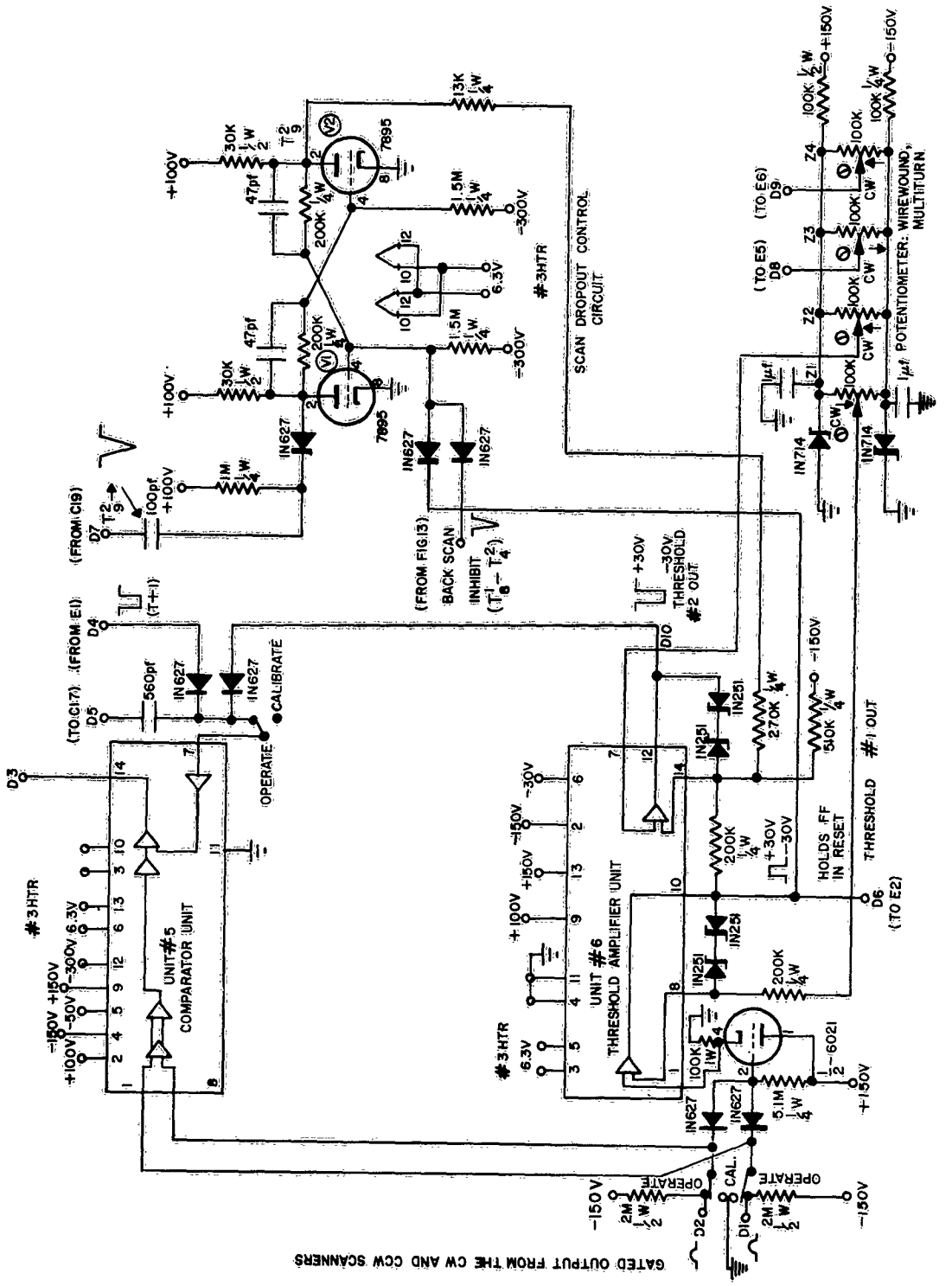


Fig. 31 - Comparator-threshold section

The logical "AND" circuit causes the grid of the buffer cathode follower to assume the lowest of the two D1 and D2 input voltages. When this voltage goes above a preset threshold (determined by the potentiometer Z1), the first amplifier output goes high at D6 and the output of the second amplifier goes low at D10. This threshold detector is the same type as that used in the event detector circuit and also uses the dual dc amplifier circuit shown in Fig. 18(b). When D6 is low, the flip-flop consisting of V1 and V2 is held in the reset condition (V1 nonconducting). A T_9^2 pulse, which occurs at the start of each scan of the delay line, is presented to the plate of V1 through a diode gate. When D6 goes high, indicating the presence of a signal at the center of the delay line, the flip-flop will then be triggered to the set condition (V2 nonconducting) by the next T_9^2 pulse. When the V2 plate goes high, the second output (D10) of the threshold detector can then go low. The D10 output combines in a logical "AND" circuit with the T+1 signal inserted at D4, and when both are low, the inhibit on the comparator circuit is released. A second input to the grid of V1 called the backscan inhibit is driven by the $T_8^1 - T_4^2$ pulse which resets the flip-flop when the scanners reach the ends of the delay line in their scanning operation. The resetting of the flip-flop causes D10 to be driven high, thus reestablishing the inhibit on the comparator. This allows the comparator to operate upon the scanner output signals over the scanning of the delay line from the center to the ends only. The flip-flop is again set at the next T_9^2 pulse if D6 remains high; this operation will continue as long as D6 remains high, thus indicating a signal which completely fills the delay line. If the signal is ragged, such that D6 goes low during a part of the scanning period, the flip-flop resets and the comparator is inhibited for the remainder of the scan period. This operation is called the scan dropout control. This minimizes random comparison outputs during periods in which the signal in the delay line contains a large amount of noise or has not reached the center of the delay line. The inhibit line to the comparator is differentiated and provides a pulse output at D5. This pulse is the E1 pulse shown in Figs. 5, 19, and 32 and indicates that the processing section is acting on a signal in the delay line. Figure 32 is the schematic diagram of the dual 150-ms multivibrator circuits for driving the output relay circuits.

The input lines D1 and D2 in Fig. 31 also connect to the comparator inputs. The comparator circuit shown in Fig. 33 consists of two cascaded difference amplifiers (V1 through V4), followed by a diode "AND" circuit and a Schmitt trigger circuit (V5). When the input voltages at D1 and D2, Fig. 31, are equal, the plate voltages of V3 and V4 in Fig. 33 will be balanced and the input to the Schmitt circuit through the diode "AND" circuit will be at its lowest value. When this condition exists, the output of the Schmitt circuit will be high provided that the comparator inhibit is removed at V6. When V6 conducts, the output of V5 is held low. If a delay line signal is present, V6 would be cut off during the scanner inhibit release period, as just described. Whenever the voltages on lines D1 and D2, Fig. 31, become equal during this period, the comparator output goes high and remains high so long as D1 and D2 voltages remain equal. The output of the comparator is clamped at ground when low.

The output of the comparator goes to a low-pass filter (see Fig. 5 and Point I6 in Fig. 34) and is then amplified by a gated amplifier. When a signal is present in the delay line, the T+1 signal is formed. This T+1 signal drives the buffer cathode follower at I4, as shown in Fig. 34. The output of the cathode follower allows the gated amplifier (which is one section of a dual dc amplifier, as shown in Fig. 18(b)) to amplify the output of the filtered comparator output. The normal output of the gated amplifier is set at a negative voltage such that the diode connected to its output is kept nonconducting. This voltage level is set by Z3 when there is no comparator output.

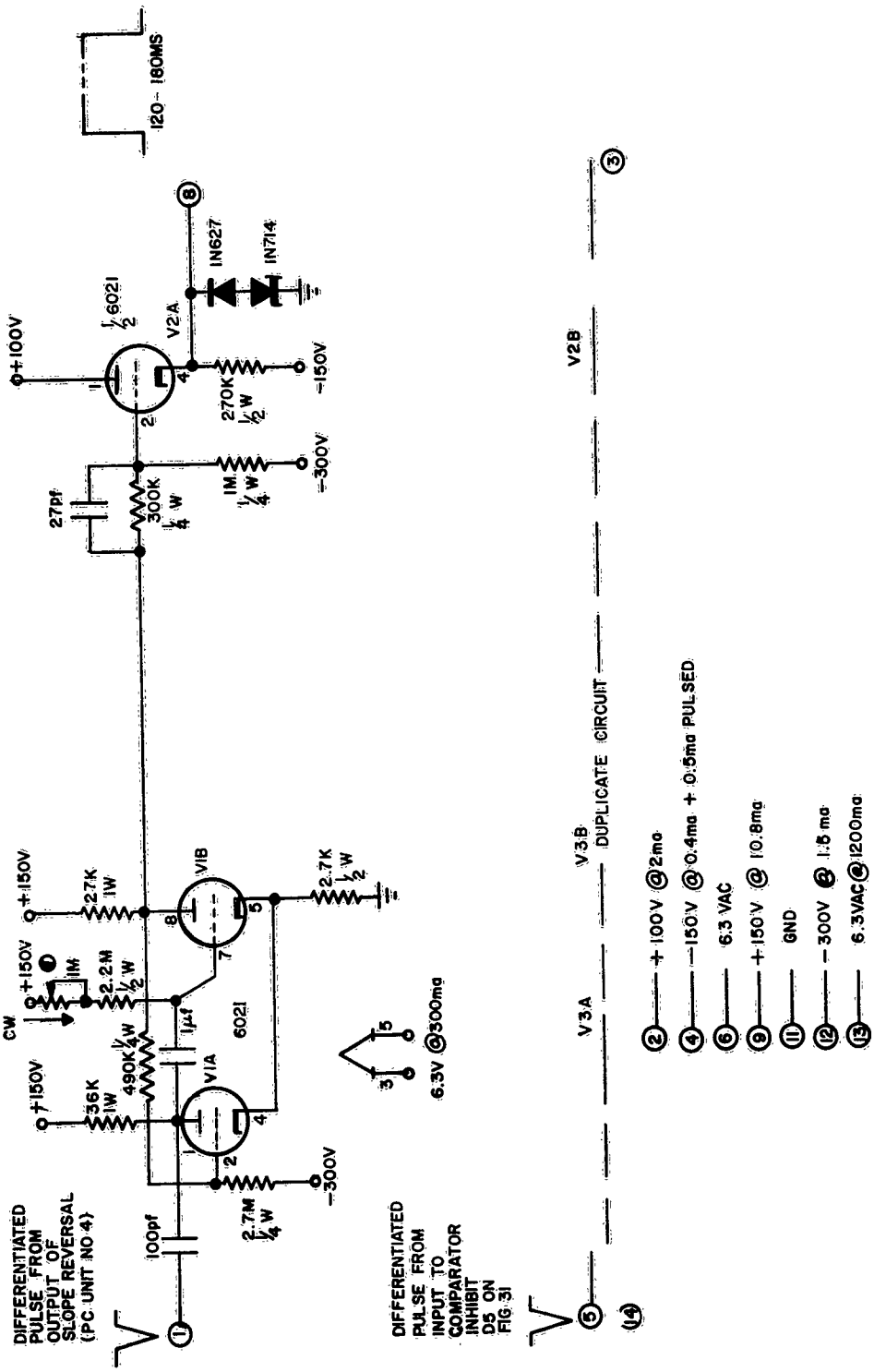


Fig. 32 - E_2 pulse driver to insertion relay unit for code 5131

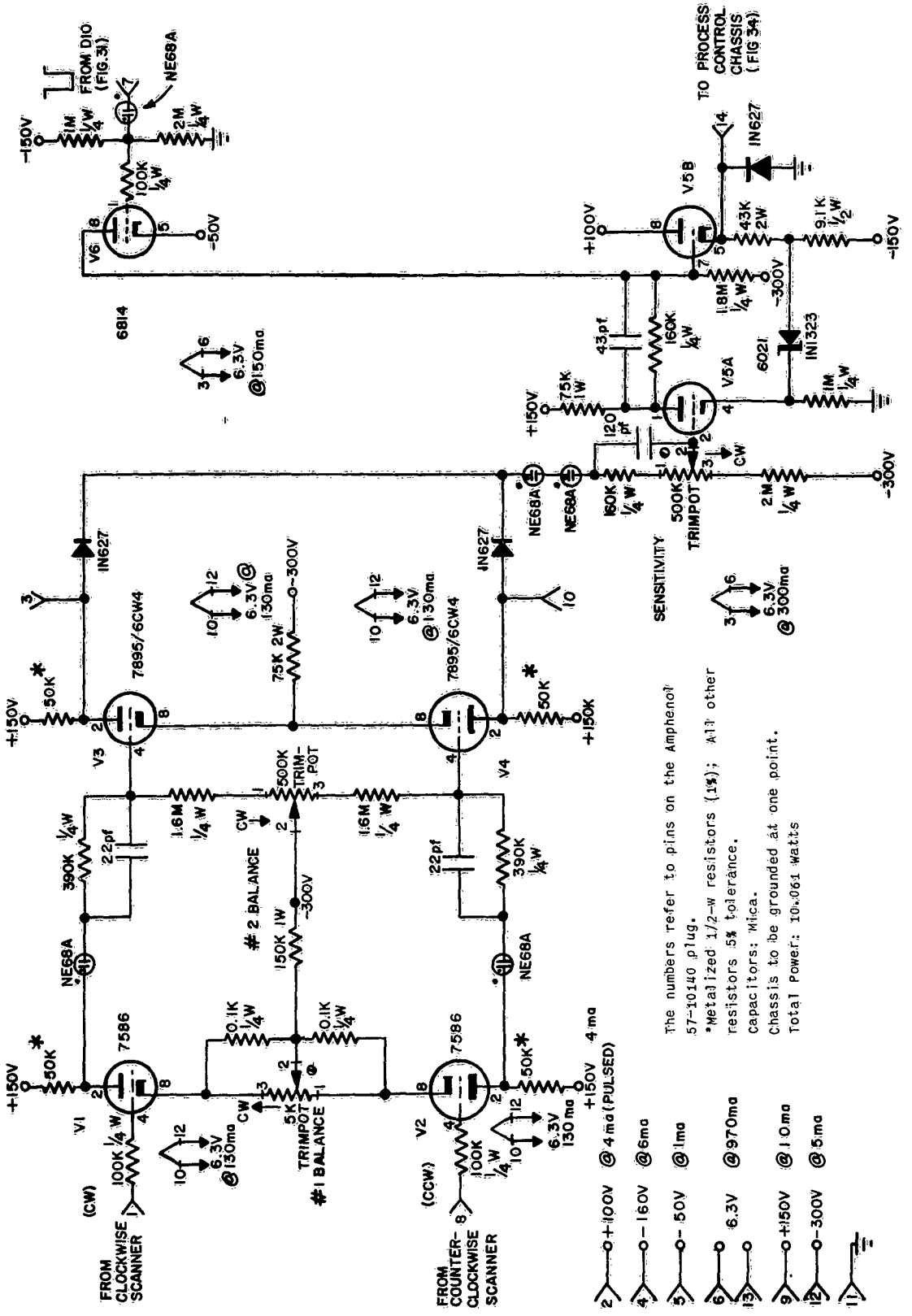


Fig. 33 - Comparator

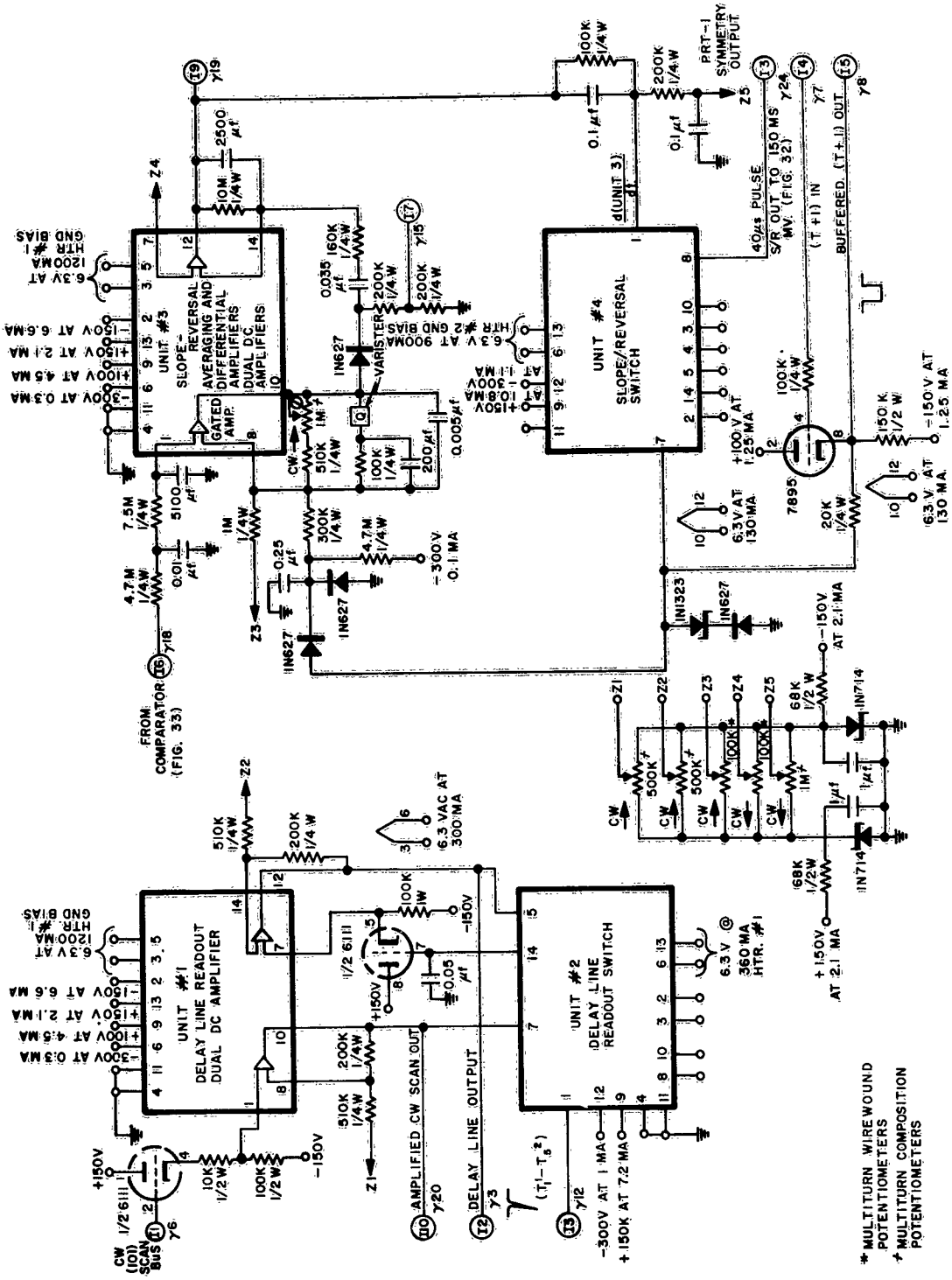


Fig. 34 - Process control chassis

When there is a comparator output, the output is averaged by the filter and then amplified. If the comparator output persists for a sufficient length of time (the signal in the delay line is symmetrical), the diode at the output of the gated amplifier conducts and drives the input to the analog differentiator. This differentiator uses the second dc amplifier in the dual amplifier unit. If the signal in the delay line is symmetrical, the output of the gated amplifier will build up smoothly to a maximum and decrease smoothly back to the zero level. The slope reversal, which takes place at the maximum output of the gated amplifier, becomes a relatively large positive-going wavefront at the output of the differentiator. This waveform is coupled to the input of a Schmitt trigger circuit in the slope reversal switch shown in Fig. 35. The slope-reversal switch unit also contains a flip-flop V3 which is set by the T+1 signal so that the flip-flop allows the input Schmitt circuit (V1) to respond on the first positive-going wavefront from the differentiator. The output of the Schmitt circuit is differentiated and triggers a one-shot multivibrator V2. The output of this multivibrator drives a buffer multivibrator (Fig. 19 and Fig. 32), which in turn causes a relay circuit in the delay relay unit (Fig. 22) to operate indicating by a switch closure that a slope-reversal took place. The output of the slope-reversal multivibrator also resets the flip-flop (V3) so that the input Schmitt circuit is inhibited until the T+1 signal ends and again reoccurs.

DELAY LINE READOUT

In order to obtain a delayed reproduction of the input signal so that we can permanently record the performance of the delay line, a delay line readout circuit was provided, as shown in Fig. 34. The output of the 101 CW scanner bus drives a buffer cathode follower at I1. This signal is amplified and drives the delay line readout switch I10 in Fig. 34. A gating pulse $T_1^1 - T_5^2$ at I3 gates the amplified scanner signal through the switch to a holding circuit at the instant that the 101 CW scanner is reading the oldest agc signal sample. The output of the holding circuit is amplified and becomes the delay line output at I2. The Unit No. 1 amplifiers are a dual unit, as shown in Fig. 18(b). The delay line readout switch is shown in Fig. 36.

In Fig. 36, the switch consists of a pair of 7586 tubes connected plates-to-cathodes at the 0.1-μf holding capacitor. The switch is controlled by one shot multivibrator MV2 which provides the sampling duration. MV2 is driven by MV1. MV1 provides the necessary delay for allowing the switch to sample during the center of the scanner dwell period.

MONITOR

The purpose of the monitor is to allow an overall system check from one central location. The monitor panel incorporates a signal simulator, a null voltmeter, and an oscilloscope switching network.

Signal Simulator

The signal simulator consists of a clock motor geared to 4 rpm which gives a basic 15-second period in 360 degrees of revolution. The output shaft is coupled to a 360-degree potentiometer and a cam. The cam operates a normally open microswitch causing the motor to run until the 360-degree cam returns to the rest position, allowing the switch to open. The microswitch is bridged by two switches: one is a mode switch, the other a start switch. With the mode switch in the normal position (open), a momentary operation of the start switch will start the motor, causing the cam and potentiometer to rotate through 360 degrees. With the mode switch closed, the motor operates continuously.

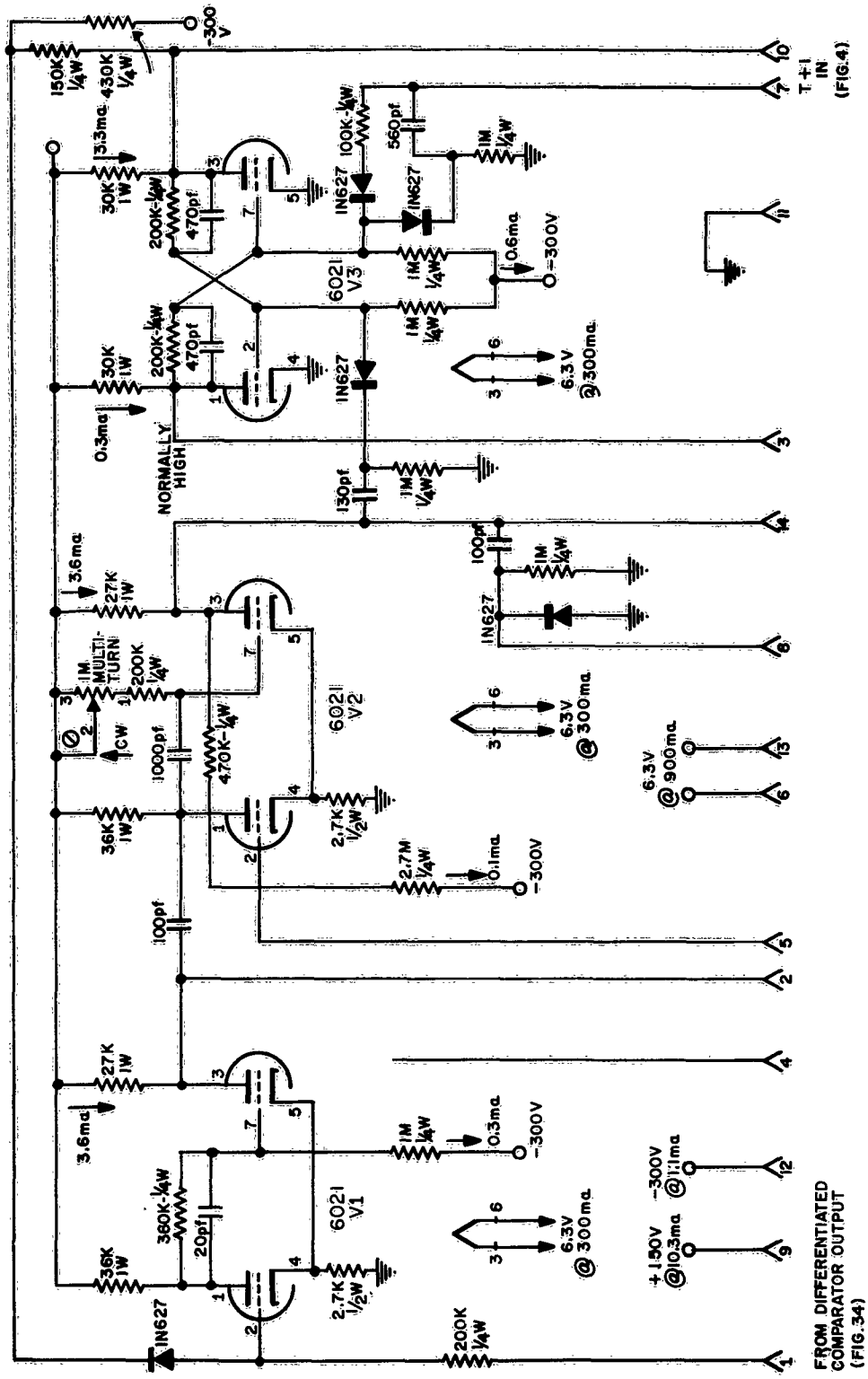


Fig. 35 - Slope reversal switching

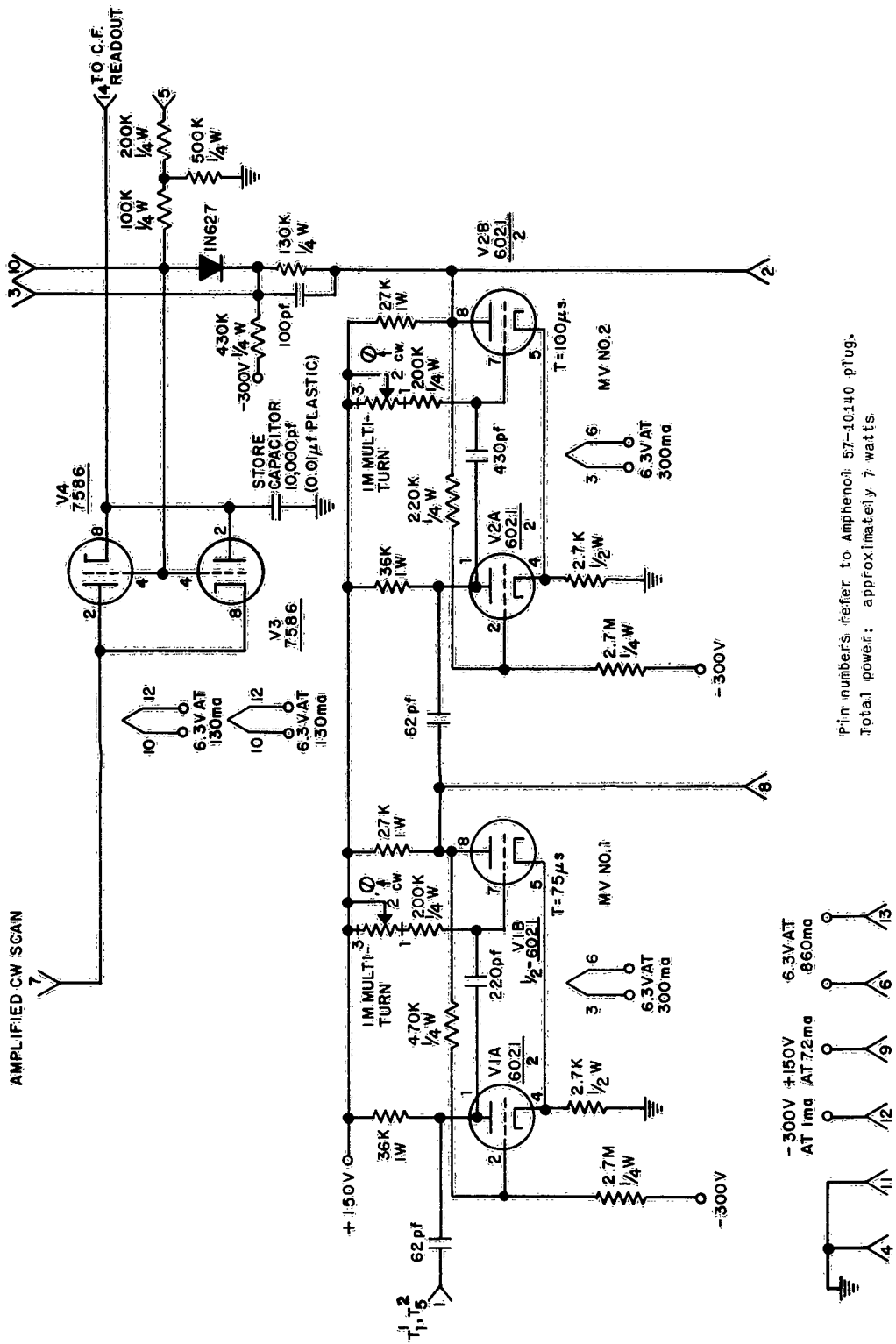


Fig. 36 - Delay line readout switch

The 360-degree potentiometer is center tapped to a bias network providing a voltage of approximately 37 volts. The ends of the potentiometer are held at ground potential. The wiper in rotating through 360 degrees and passes from zero potential through 37 volts back to ground in 15 seconds, thus providing a triangular waveform. The wiper output is fed into a six-position switch, which contains a series of Zener reference and biasing diodes (see Fig. 37). The breakdown values of the reference diodes were chosen to provide the proper signal time base. The original triangular waveform is modified by preserving that which exceeded a preset dc level. The removal of the dc offset is accomplished through a cathode follower biased to provide zero output. The net effect is a group of six signals of increasing duration and amplitude, each simulating a class of satellite responses.

Null Voltmeter

The system requires seven different voltages: -300, -150, -50, -6.8, +18, +100, and +150 volts. Since the unit contains several dc amplifiers, the voltage values are critical and must be kept within one-half of one percent for proper operation. A passive null balance meter was chosen (see Fig. 38). The meter was designed for two reference levels, +5.6 and -5.6 volts. The levels were provided by two 1N708 Zener diodes biased from the +150 and -150 volt supplies. It was found that a variation of up to ±15 percent in either of the two supplies did not measurably affect the level of the respective reference voltage. A zero center 100-0-100 microampere meter movement was inserted between the reference voltage and its respective comparison voltage. The positive voltages from the system were summed together on a precision resistor voltage divider. Ratios were chosen so that each voltage alone would produce exactly 5.6 volts at a tap near the bottom of the divider. Since each voltage was related to this tapped point by a fixed constant ratio, a variation in any voltage by a fixed percentage would produce a standard deflection on the meter.

This method was also used for the negative voltages. The meter movement was protected by bridging the movement with two 1N100 germanium diodes, which have a forward breakdown of 0.2 volt. A variation of ±3.5 percent in any voltage level would correspond to full-scale deflection of the microammeter.

Oscilloscope Switching

The monitor panel was provided with a 24-position switch to which were connected taps from several monitoring points in the symmetry recognition circuitry. Each line was equalized in order to require the fewest possible oscilloscope settings. The T_9^2 pulse provided external synchronization for each position. The monitored functions are listed in Appendix B.

RESULTS

System Technical Performance

During the period October 30 through November 4, 1961, the installation and checkout of the Symmetry Recognition II equipment was conducted at San Diego SPASURSTA. The station personnel were given a brief period of instruction and were provided with a complete set of schematics and block diagrams. Once each day, a SPASURSTA technician operated the built-in simulator to check the system thresholds. He performed a simple adjustment if the response patterns on the Sanborn recorder justified a change. Minor resets of this nature were made after approximately each 200-hour period.

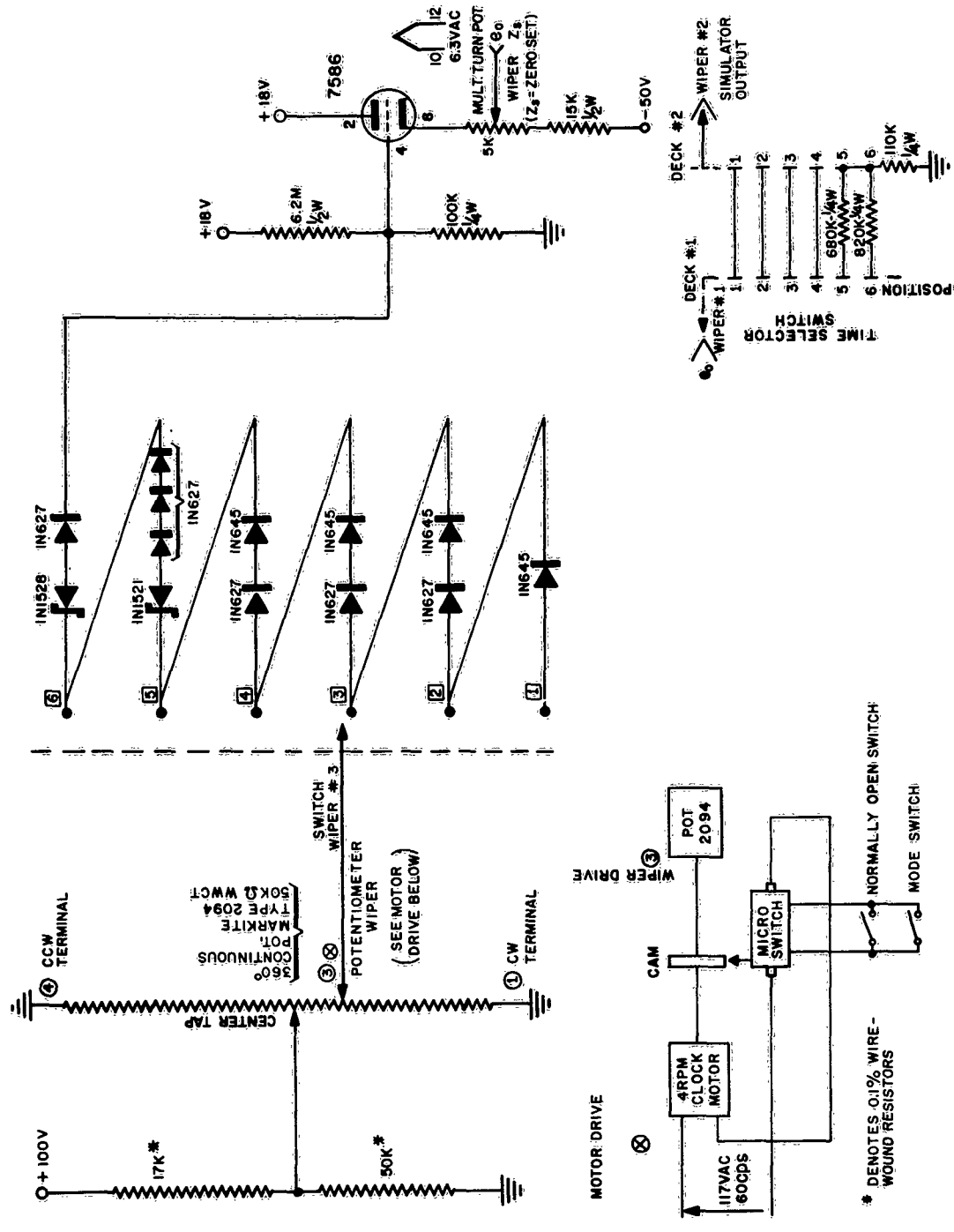


Fig. 37 - Monitor panel simulator

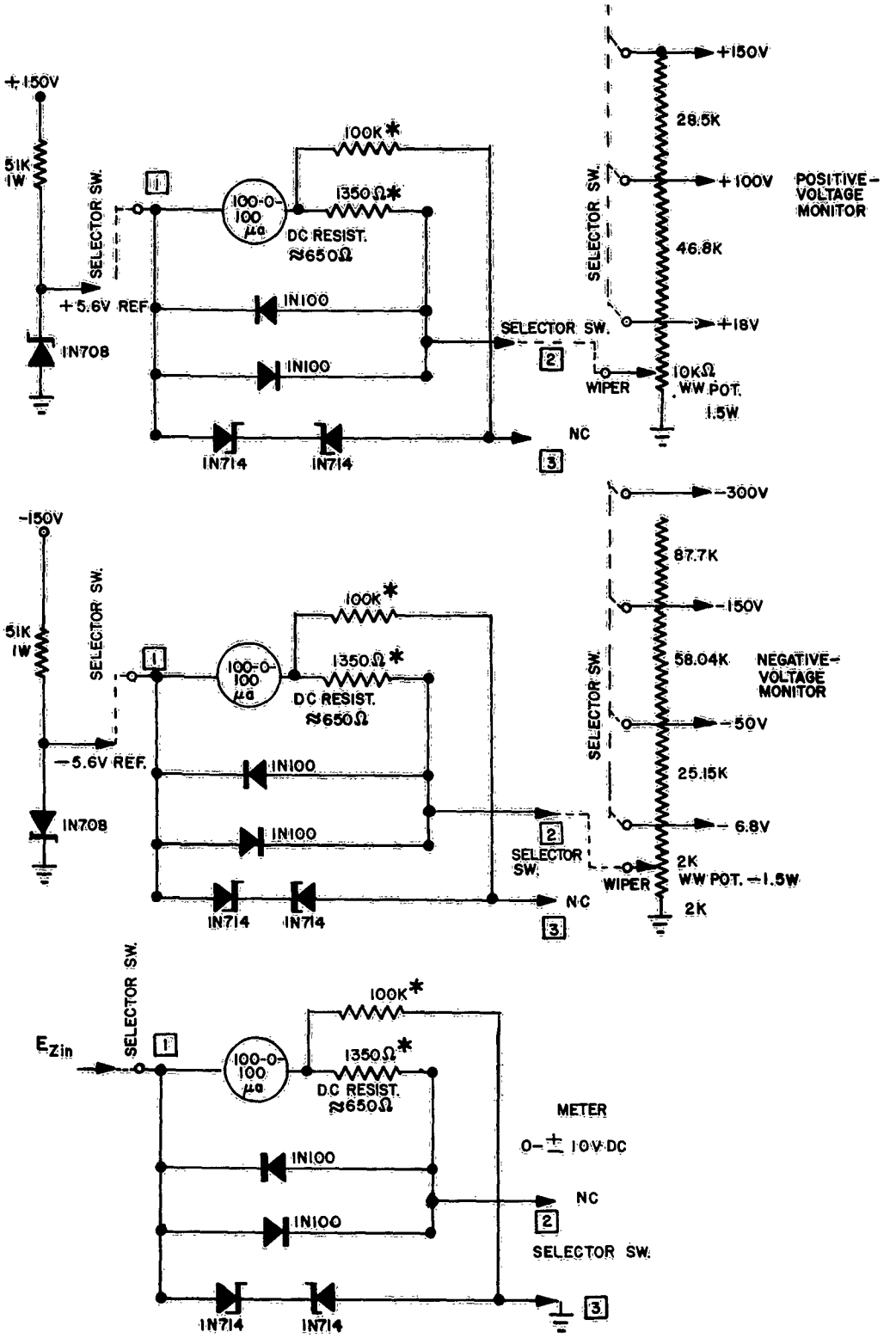


Fig. 38 - Monitor panel null voltmeter

Shortly after 1000 hours of satisfactory operation, the delay-line-readout circuit performance degraded to the point where the routine check of thresholds could not be continued. After several phone calls and whatever spare time effort that the station personnel could apply, a partial restoration of the delay line readout was accomplished. The resetting of thresholds was again attempted, but was not entirely satisfactory. Following several further attempts to advise the San Diego personnel by telephone, the recommendation to discontinue operation of the equipment was made on February 20, 1962. Excellent cooperation was extended by the San Diego SPASURSTA personnel, who devoted considerable spare time attempting to locate and correct the fault.

System Operational Performance

The installation of the Symmetry Recognition II equipment was completed on November 5, 1961. Assuming the adjustments were optimum at this time, a period of 10 hours was arbitrarily selected from the Sanborn record for the following day, November 6. Subsequent review of records received for the succeeding three weeks displayed a performance level which had not changed measurably from that on November 6.

Between 0614Z and 1617Z on November 6, 53 satellite passes were verified by NAVSPASUR, Dahlgren, Va. After removing responses due to calibration signals and radiating satellites, the system performance was scored as follows:

Alert Type		
A	Symmetry Recognition Response to verified satellite signal	20
B	Symmetry Recognition Response to signals not verified as satellites	14
C	No Symmetry Recognition Response to verified satellite signals	33
D	No Symmetry Recognition Response to nonsatellite signals	39
	TOTAL ALERTS	106

It can be seen that 32 percent of all signal alerts were called symmetrical. This is less than the call rate represented in Figs. 2 and 6 in NRL Report 5665 (Ref. 3). It is very disturbing to note that for the 53 verified satellite passes, only 20 were recognized by the Symmetry Recognition System II. A further study into the reasons for this apparently poor performance revealed the following categories, and the numbers in each:

Alert Type		
C-1	Satellites missed by Symmetry because virtually no signal was apparent in the Sanborn record of the selected agc	25
C-2	Satellites missed by Symmetry because short duration signal was distorted by the comb-filter switching action	7
C-3	Satellite missed by Symmetry because of a combination of rapid-fluctuation (1961 Omicron 14), low-level, and short-duration of the signal	1
	TOTAL TYPE C ALERTS	33

A study of the 14 Type B alerts, or so-called "false alarms," showed strong symmetry in each instance. The characteristics observed in four signals suggest the possibility that the responses were due to a satellite located outside the normal prediction region for the San Diego SPASURSTA. These have been labeled Type B-1. Inevitably, a few responses due to anomalies, such as overdense meteor trails, will have portions of their signatures which display enough symmetry to correspond to a satellite. These must be classified as false alarms, and the ten of this variety have been designated as Type B-2.

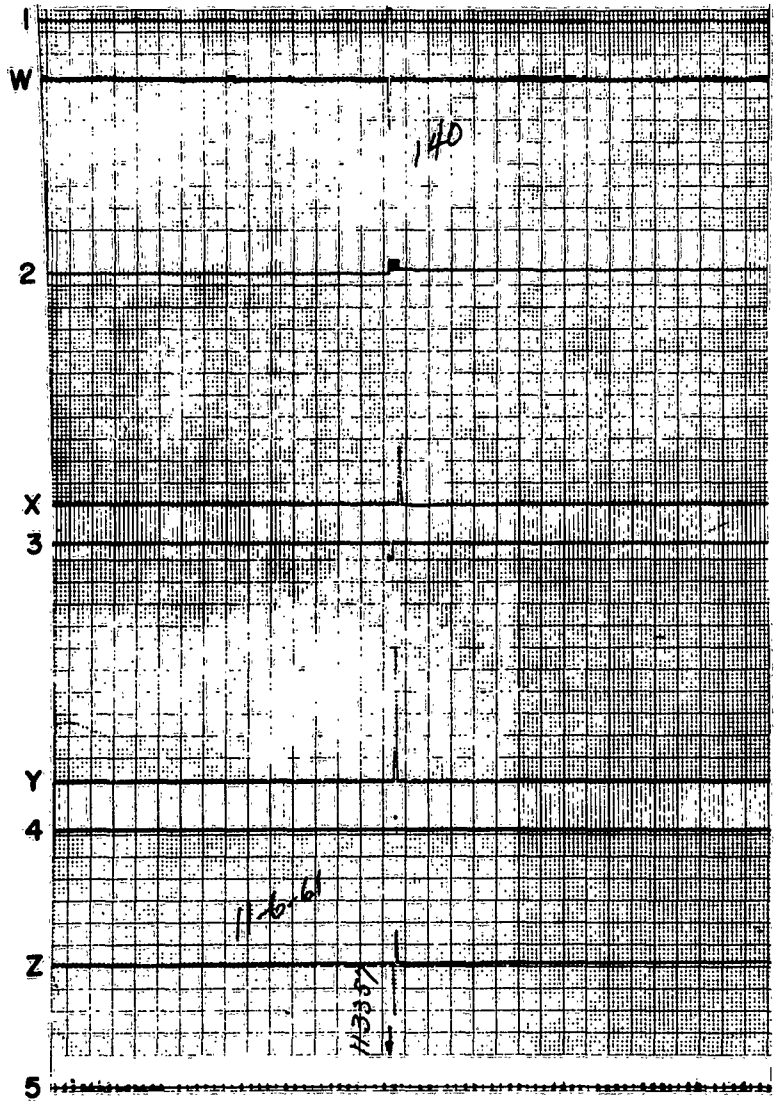
Figure 39 shows examples of the Symmetry II performance under a wide variety of operating conditions. Figure 39(a) is a one-millimeter-per-second Sanborn record of a classical satellite signal with a duration just under one second and a normal symmetry response. The selected agc, a negative-going signal on line W, is reproduced at the output of the delay line two seconds later on line X. Line Y shows the degree of symmetry, reaching its maximum one second after the peak of the signal enters the line, as diagrammed earlier in Fig. 2. Line Z is the differentiation of line Y, helping to define the instant of slope reversal at the center of the signal, and also enhancing the ability to discriminate against nonsatellite signals. The event pens show the comb-filter alert pulse on both lines 1 and 3. As received from the ADDAS equipment, an alert must be 0.2 second or longer to operate these event markers. Line 2 is the E-1 pulse, enabled by the alert and operated by the threshold detectors in the delay line. The E-1 pulse signifies that the symmetry comparison process is induced by the presence of some signal in the line. Line 4 is the PRT-1, the symmetry output decision pulse. Line 5 is the SPASUR time code, permitting correlation with other system records, especially the observations confirmed by NAVSPASUR. This code is also tabulated in Appendix C.

Figure 39(b) is typical of a low-altitude polar orbit. The PRT-1 symmetry response was given, even though a portion of the signal was omitted by the comb-filter switch delay. Figure 39(c) is one type of radiating signal. Note that only one PRT-1 is given, near the center of the signal. Figure 39(d) shows a radiating satellite continuing for over 2-1/2 minutes. The PRT-1 responses precede the peak by only 10 seconds, and render only six responses.

Figure 40 shows a B-1 type response not reported as a valid observation, but possibly of satellite origin. Also on Fig. 40 a Type C-1 case is encountered. A broad 10-second signal does not exceed the level of the background noise, and hence cannot be measured for symmetry. Figure 41 shows five further examples of Type C-1 verified satellites which evidence no selected agc for numbers 28, 130, 154, 149, and 122. Figure 41(b) also includes a nine-level SPASUR threshold calibration starting at -136 dbm, then -139 dbm, and thereafter descending 1 db each step. On Fig. 41(c) an example of Type C-2 is shown wherein number 135 is a strong, but short, signal that was so distorted as to lose its symmetry, thereby preventing a PRT-1 response. Also of interest are two nearly coincident meteors, both of which were rejected by symmetry. Note the similarity of these delay line signals with that of satellite 135. Figure 42 is a Type D example of a large meteor response which was rejected for the lack of symmetry.

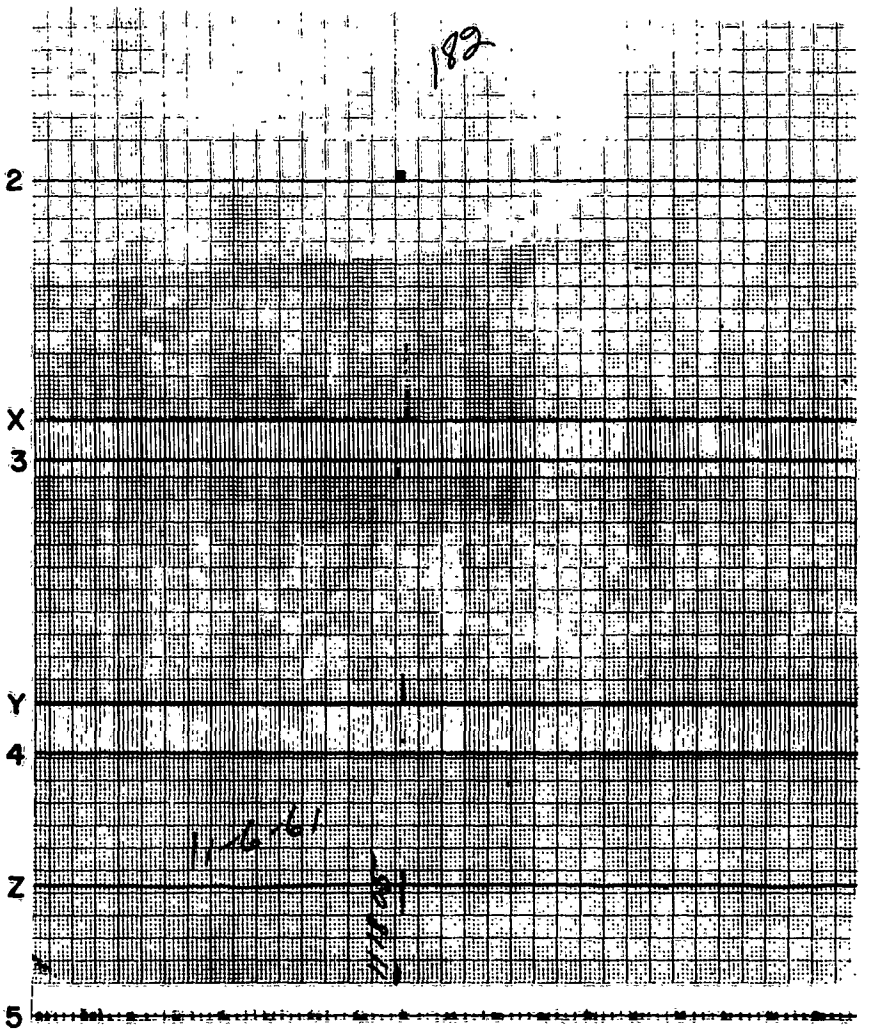
CONCLUSIONS

In comparison with the breadboard Symmetry Recognition System reported upon in NRL Report 5665, the Symmetry Recognition System II technical performance showed improvements in the signal-to-noise ratio of the delay-line output. The limited availability of maintenance effort prevented extensive reliability studies, but an initial run gave over 1000 hours of service before the first failure occurred, thus forecasting a minimum of repairs. Serviceability was simplified through the monitor facilities and the interchangeable plug-in units. Design improvements reduced the space required from four standard racks to one cabinet and effected a power reduction from 4.5 kw down to 1.2 kw.



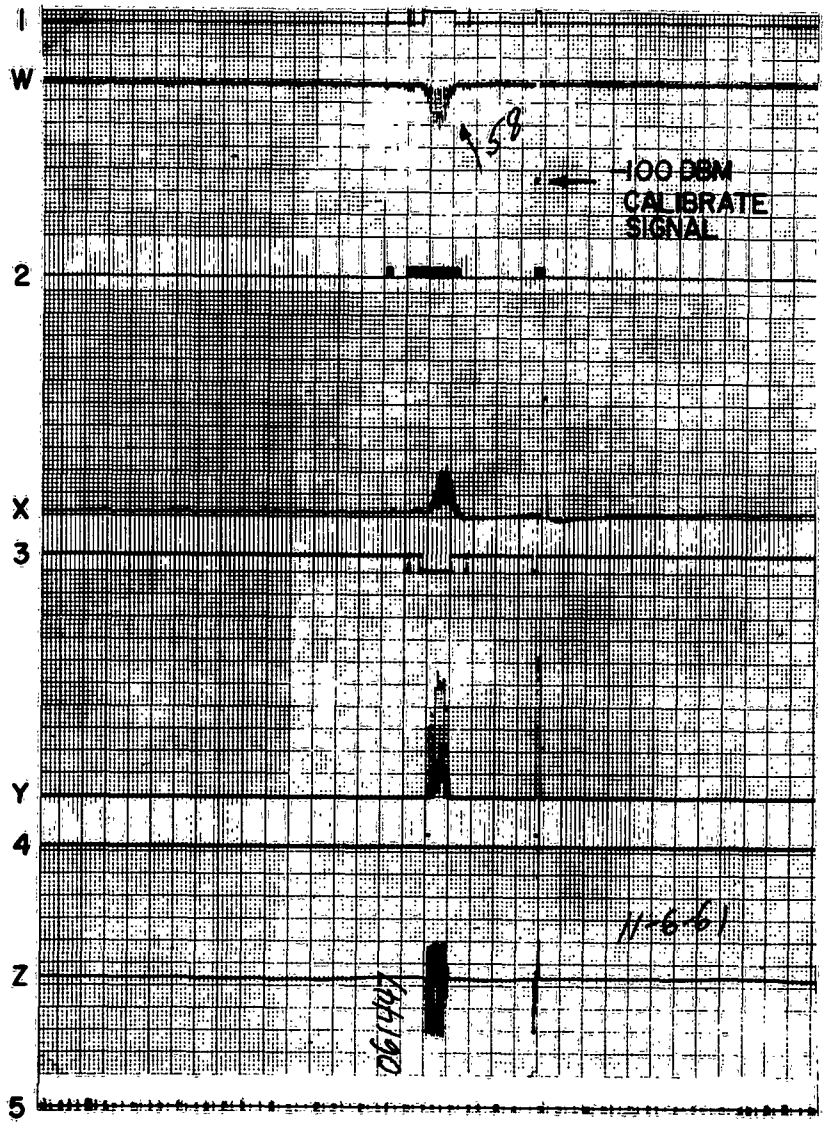
(a) Classical satellite signal with normal symmetry response

Fig. 39 - Examples of satellite detection using the Symmetry II System



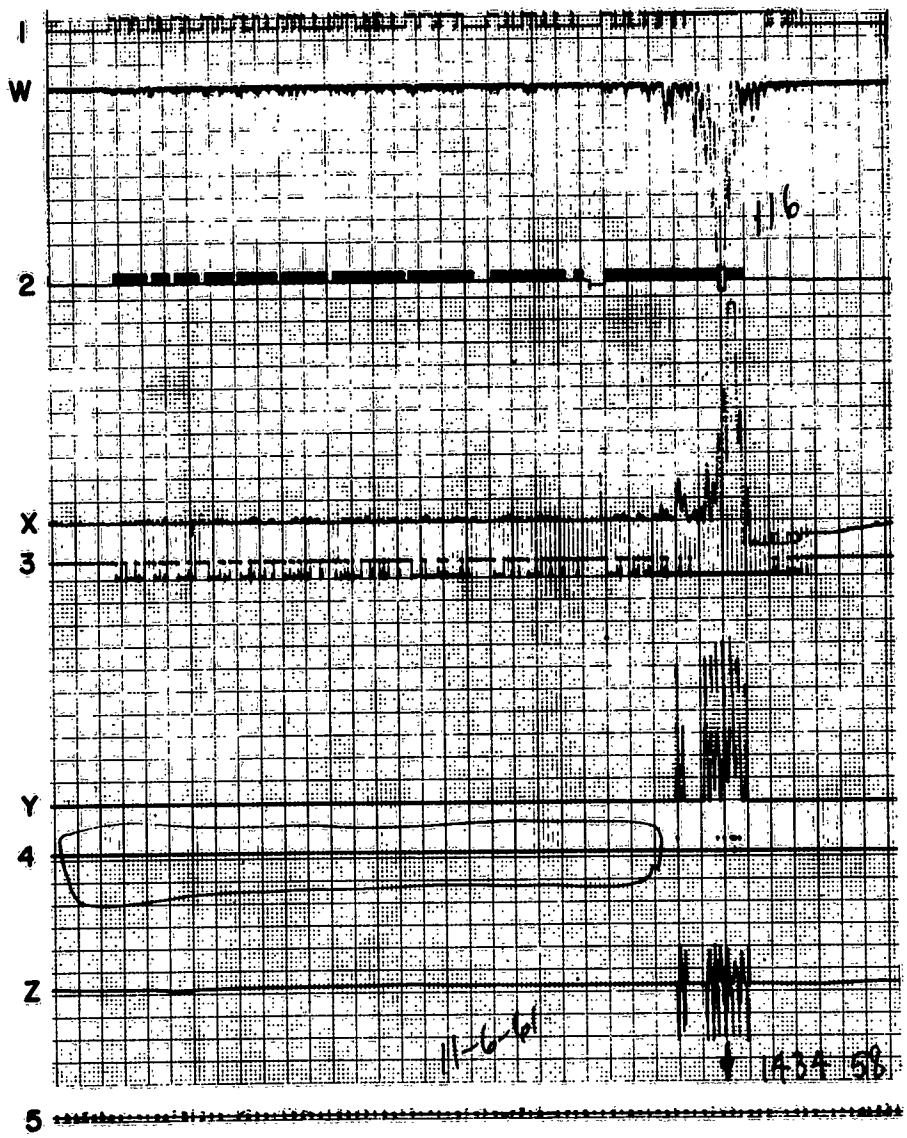
(b) Short-duration, large-amplitude response typical of low-altitude polar-orbit satellite

Fig. 39(continued) - Examples of satellite detection using the Symmetry II System



(c) Signature probably due to distant satellite radiating on 108 Mc and tumbling at about 48 rpm

Fig. 39(continued) - Examples of satellite detection using the Symmetry II System



(d) Radiating satellite response continuing for over 2-1/2 minutes

Fig. 39(continued) - Examples of satellite detection using the Symmetry II System

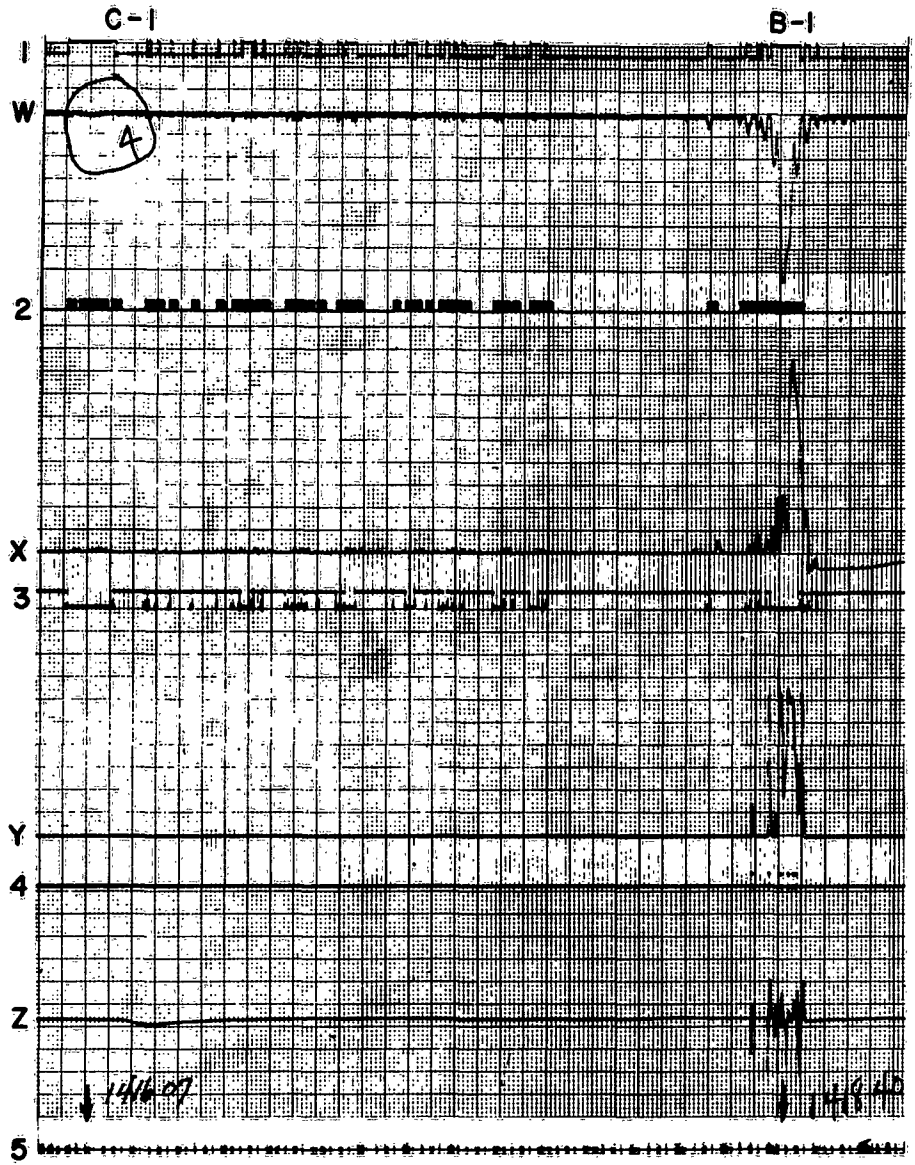
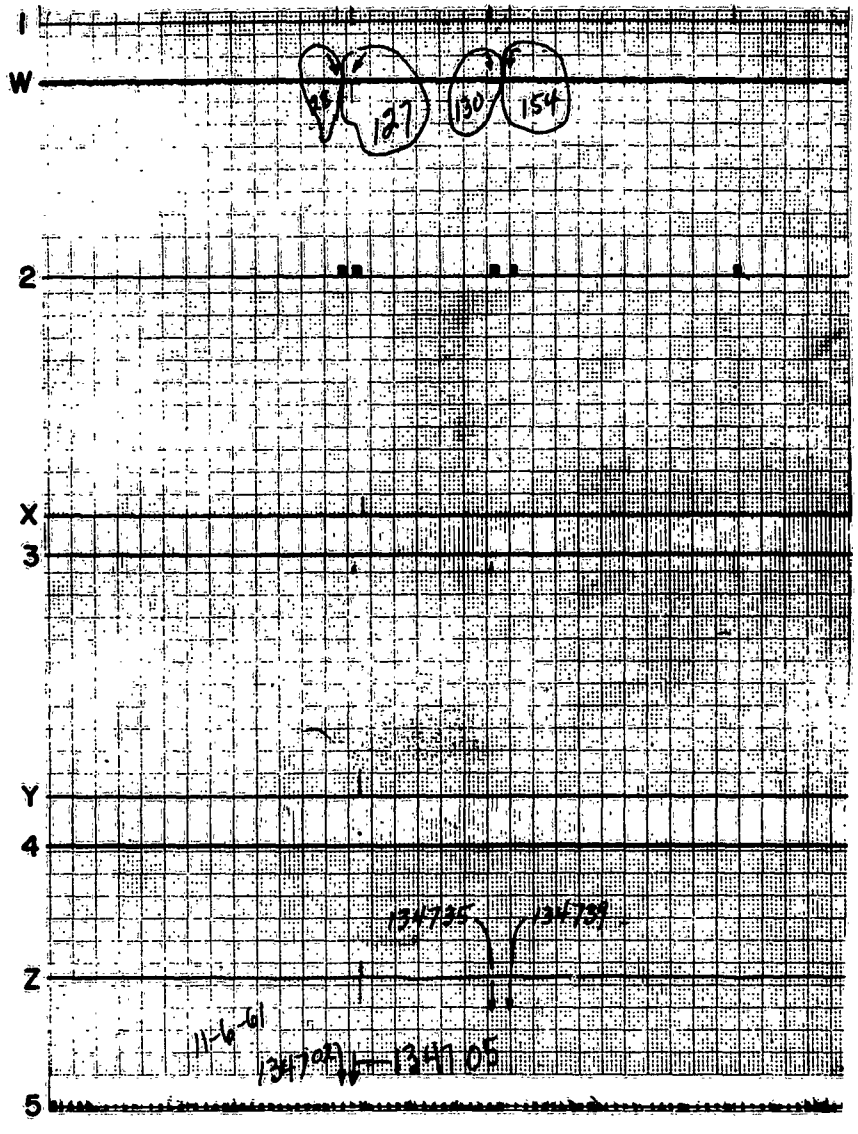
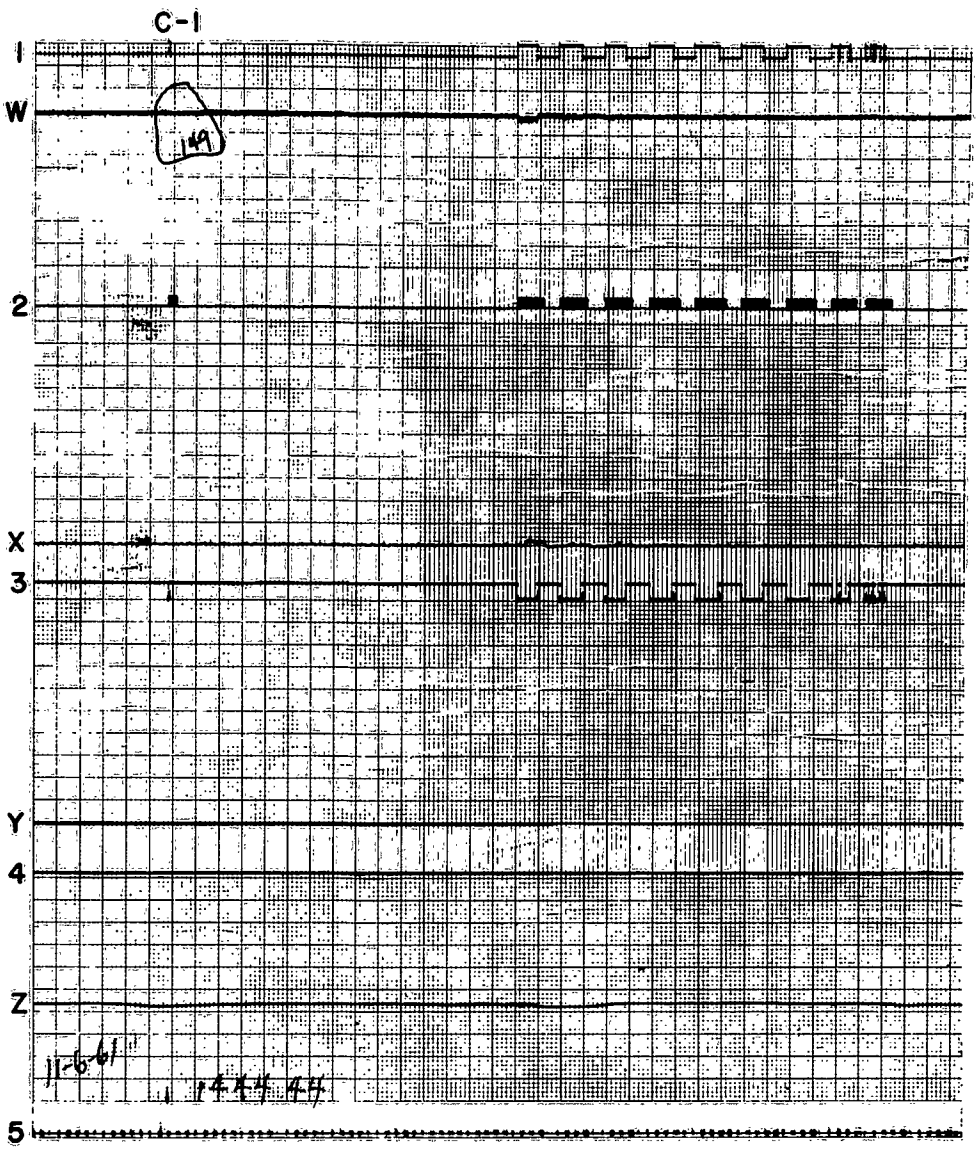


Fig. 40 - A broad, low-level (Type C-1) satellite response (labeled 4) with an agc response below the Symmetry Recognition H threshold. Immediately following are unconfirmed (Type B-1) responses which continue for over 2-1/2 minutes. The source is probably a satellite radiating on 108 Mc and crossing the SPASUR line at an angle near the horizon.



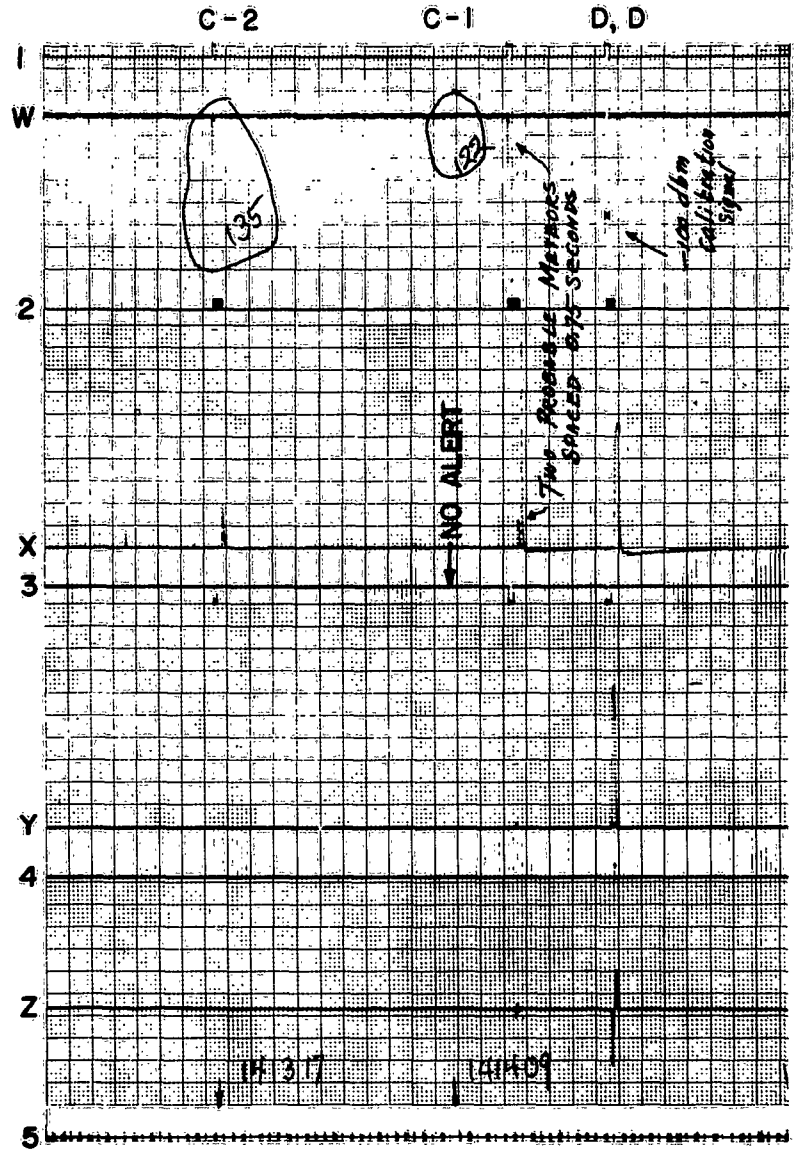
(a) Three satellite passes detected by the narrow-band comb-filter system. Insufficient agc response prevented symmetry recognition processing. A fourth satellite (127) gave normal responses

Fig. 41 - Examples of Type C-1 and C-2 alert signals



(b) Low-level response 149 is followed by a nine-level SPASUR threshold calibration representing -136, -139, -140, -141, -142, -143, -144, -145, and -146 dbm

Fig. 11(continued) - Examples of Type C-1 and C-2 alert signals



(c) Satellite response 135 has been distorted by the narrow-band comb-filter switching so as to appear as a meteor, causing a rejection by symmetry recognition

Fig. 41(continued) - Examples of Type C-1 and C-2 alert signals

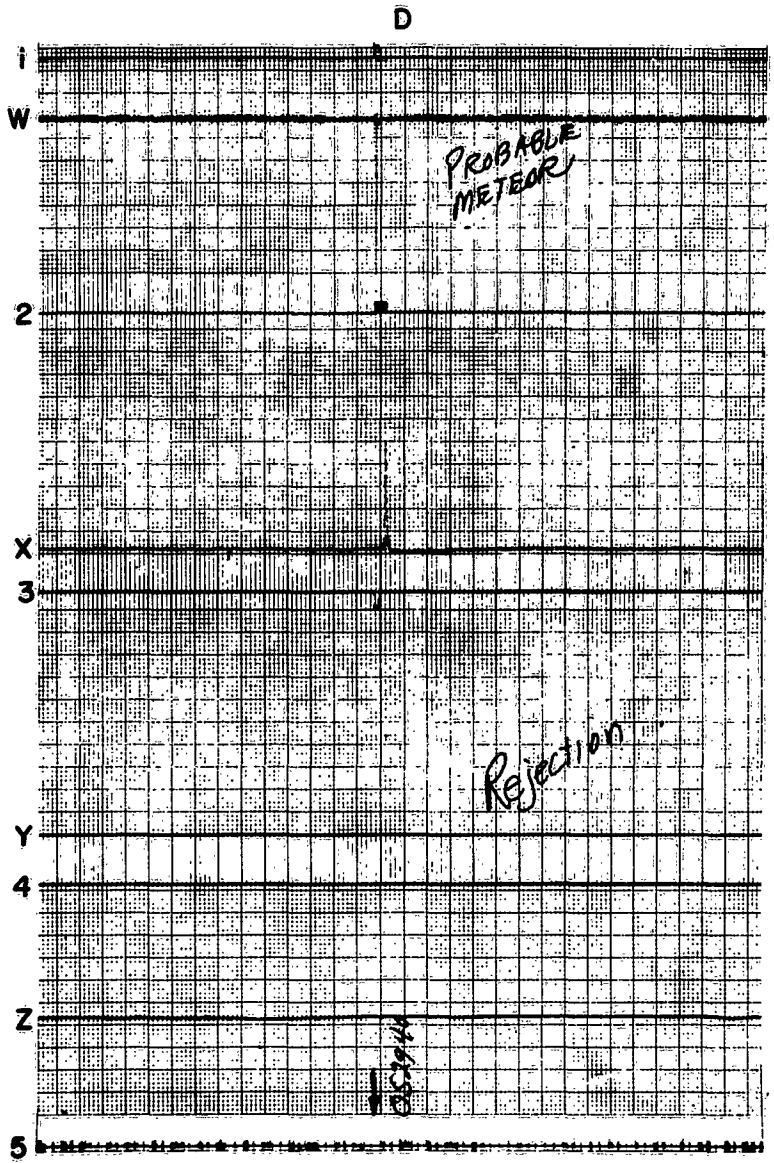


Fig. 42 - Typical rejection of a probable meteor by the Symmetry Recognition System II

In terms of operational performance, the Symmetry Recognition II (SR-II) equipment achieved the objective for which it was designed. It measures the degree of symmetry of signals lying between 0.2 second and an upper limit of from 5 to 10 seconds and having peak amplitudes from about -130 dbm to -100 dbm and larger. The equipment reliably classifies each signal according to the threshold limits established by the operator.

Measured in terms of its reliability in identifying satellites by their agc signatures while discriminating against all nonsatellite signals, the characteristics of the system supplying the agc signal have a determining effect. The original Symmetry Recognition equipment installed at Ft. Stewart, as reported in NRL Report 5665, recognized 37 percent of all events. Of those events called symmetrical, 10.8 percent were verified satellites, the latter representing 90 percent of all satellites verified for that period.

The SR-II installation, operating with the narrow-band comb-filter installation in San Diego, recognized 34 percent of all alerts. Of these PRT outputs, 54 percent were verified satellites, the latter representing 37.8 percent of all satellites verified for that period. False alarms were reduced from 89 percent at Ft. Stewart to 46 percent at San Diego. While technical improvements in the symmetry recognition equipment favored the SR-II performance somewhat at San Diego, the major differences were caused by the changes in the SPASUR system. A 12-db advantage in the alert and phase channel sensitivity over the selected group agc signal left 47 percent of the verified satellites below the operating level of the SR-II equipment, which is limited by the external noise level to about -130 dbm. An additional 13 percent of the verified satellite signals were sufficiently distorted by the switching action of the comb-filter to destroy their symmetry and cause their rejection. Of the 40 percent remaining verified satellites, only one, representing 5 percent of this group, was not recognized.

It appears that the current reliance upon the highly sensitive phase information, the doppler signals derived from the comb-filter, and the use of triangulation observations has brought the SPASUR system performance to a level that would enjoy little improvement due to the addition of pattern recognition information based upon the group-selected agc.

RECOMMENDATIONS FOR FURTHER DEVELOPMENTAL EFFORT

Some consideration should be given to methods of further simplifying and improving the techniques employed in the Symmetry Recognition II equipment if additional units are required. For example, by differentiation of the agc at the input, it appears that many benefits should occur. The amplitude range of low-frequency analog values presented for storage in the delay line could be extended, and requirements for a dc drift corrector would undoubtedly be circumvented. A 2:1 increase in time resolution would be necessary in the delay line to handle the higher frequency components which would result, but this is desirable for other reasons cited earlier. In operation, the delay line scanners would be resistor-summed to permit mirror images of the differentiated symmetrical signals to cancel as a measure of symmetry. All differentiated symmetrical signals would cancel in this manner as they pass the center of the delay line, whereas an unbalance would be present at all times, except for occasional transients during zero crossings for nonsymmetrical signals. A further benefit would occur in the processing of square-wave calibrate pulses, which would produce only two spikes having practically zero symmetry.

Some improvement in the operational performance should be obtained by reverting to the use of the wide-band agc. This would eliminate the C-2 type of missed satellite distortion caused by the comb-filter switching action, along with an undetermined but small difference in sensitivity. There appears no reasonable way to obtain an agc signal with the full sensitivity and signal-to-noise ratio of the alert system.

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2. Fluhr, F.R., "Subminiature Package Units," NRL Memorandum Report 461, May 3, 1955

3. McLaughlin, D.J., Fluhr, F.R., Kurner, C.J., Dahl, W.D., and Grady, D.F., "Satellite Signal Analysis and Classification," NRL Report 5665 (Confidential Report, Unclassified Title), Oct. 23, 1961

APPENDIX A

CORRECTION OF GAIN ERRORS AND OFFSET VOLTAGES DURING SIGNAL INSERTION PROCESS

The insertion driver used to put the signal into the Symmetry Recognition System II delay line uses the condition that small offsets and gain variations of a circuit placed within the feedback loop of an operational amplifier are reduced by the reciprocal of the amplifier open-loop gain. By this means, the storage cathode-follower errors are minimized. In Fig. A1 is shown a functional diagram of the overall error minimization method. The switching used to insert the sequence of cathode followers has been omitted, and it is assumed that the switches will be closed long enough so that the dc steady state is reached by the circuit. This holds in practice because the insertion period is greater than 4 milliseconds and the time constant of the charging circuits is approximately 100 microseconds so that a settling period for 10 time constants is 1 millisecond. From Fig. A1,

$$E_a = -ACV + BCE_s \text{ and } V = \left(\frac{R_1}{R_1 + R_2}\right) E_o.$$

Since

$$E_o = KE_a + E_b, \text{ then } E_o = K\left[BCE_s - ACV\right] + E_b, \text{ or}$$

$$E_o = KBCE_s - \frac{KACR_1 E_o}{R_1 + R_2} + E_b.$$

This may also be written

$$E_o = \frac{KBCE_s + E_b}{1 + \dfrac{KACR_1}{R_1 + R_2}} = \frac{E_s + E_b/KBC}{\dfrac{1}{KBC} + \dfrac{A}{B}\left(\dfrac{R_1}{R_1 + R_2}\right)},$$

where the symbols have the following meanings:

E_s = input signal

E_a = output of the amplifier

K = gain of storage cathode follower ($K \leq 1$)

E_b = bias offset voltage of storage cathode follower

$+A$ = gain of negative input of amplifier

$-B$ = gain of positive input of amplifier

$-C$ = gain of output section of amplifier

V = input voltage to negative input of amplifier.

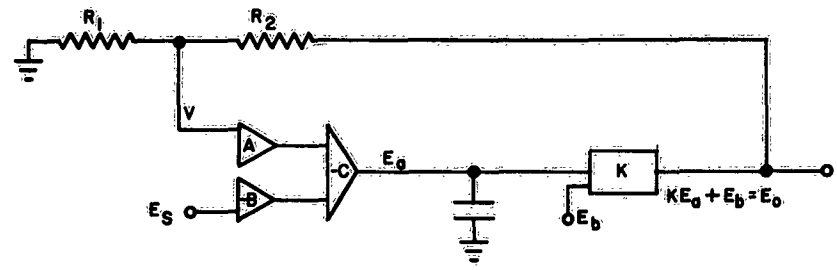

Fig. A1 - Insertion driver circuit

The expression for E_o shows that the bias offset voltage E_b is reduced by the factor $1/KBC$. By making KBC very large (several thousand in a practical case, or, in the limit, approaching infinity) then:

$$E_o \approx (B/A)\ (1 + R_2/R_1)E_s.$$

In practical operational amplifiers, the gain C is made very large (greater than 1000), and $B \geq A$ so that

$$E_o \approx 1 + (R_2/R_1)E_s.$$

APPENDIX B

MONITORING FUNCTIONS SELECTABLE FOR OSCILLOSCOPE PRESENTATION

Selector Position*	50 Pin No.	A Position (Bank No. 1)	Location	50 Pin No.	B Position (Bank No. 2)	Location	Bank No. 3
1	1	Clock Pulse	104, 119 F2	-	-	-	T_9^2
2	10	Raw agc	102, 01	11	Preamp agc	103, 122 H_1	
3	11	Preamp agc	103, 122 H_1	12	Amp agc	06, H_2, C15	
4	13	99 ccw	100, 119 D_2	14	101 cw	101, 119 D_1	
5	12	Amp agc	06	15	Delay line out	02, I_2	
6	16	1st threshold	E_2, D_6	13	99 ccw	100, 119 D_2	
7	17	2nd threshold	D 10, 119, 5	14	101 cw	101, 119 D_1	
8	17	2nd threshold	D 10, 119, 18	18	Comp out	I_6, 119 D_3	
9	12	Amp agc	06	19	Event out	E_4, 09	
10	20	T + 1	I_5, 122 (8)	21	S/R out	I_8, C_{16}	
11	19	Event out	E_4, 09	20	T + 1	I_5, 122 (8)	
12	22	$T_8^1 + T_9^2$	F_1	23	$T_8^1 + T_4^2$	113B, 108	
13	24	$T_9^1 + T_4^2$	I_3, 113C	25	T_0^2	113E	
14	25	T_0^2	113E	26	T_9^2	113F, F5	
15	27	T_0^4	114H (F6)	-	-	-	
16	28	Gnd					
21 { BNC, BNC, BNC } in back	29	A probe	} for miscellaneous servicing				
	30	BB probe					
	31	Sync probe					
Use externally set scope controls	2	BX-1		3	BX-2		
	4	BX-3		5	BX-4		
	6	BX-5		7	BX-6		
	8	BX-7		9	BX-8		

*There are 24 positions on the selector switch.

APPENDIX C

KEY TO RECORDINGS OF SELECTED AGC SIGNALS AND SYMMETRY RECOGNITION SYSTEM II RESPONSES

Event Marker Pens

Pen 1: Symmetry Recognition II event. This pen may operate from internal threshold decision circuit, or it may be externally controlled. The output is designated AGC-3 when delivered to ADDAS. In all cases presented here, it was externally controlled by the alert pulses of 0.2-sec length or greater, as determined by the ADDAS.

Pen 2: Symmetry Processing Signal, designated E-1 to ADDAS, resulting from delay line scanner threshold operation being "AND" gated with the AGC-3 event. Its purpose is to show ADDAS that a signal is being analyzed in the delay line.

Pen 3: AGC-3 event pulse as received from ADDAS, where it is derived from an alert pulse which has exceeded 0.2-sec duration.

Pen 4: PRT-1 response delivered to ADDAS signifying that the signal peak, occurring one second previously, was symmetrical, having exceeded that value for which the SR-II is adjusted.

Pen 5: SPASUR time code repeated at 10-sec intervals. All recordings were taken at 1 millimeter per second.

Analog Channel Pens

Pen W: Selected Group AGC provided by the narrowband system group, within which the alert signal originated. An increasing signal is in the negative, or downward, direction.

Pen X: Delay Line Output. Signals on W are reproduced here two seconds later. The dc level corrector causes a reference level shift on prolonged signals which restores in about 15 seconds.

Pen Y: Averaged Comparator Output. This trace measures the degree of symmetry about the delay line center.

Pen Z: Differentiation of the signals appearing on Y provides the slope-reversal signal employed in defining the center of a symmetrical signal and discriminating against many nonsatellite signals not possessing the rapid slope-reversal.

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It is concluded that recent design advances in the SPASUR system have minimized the requirement for pattern recognition processing.

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